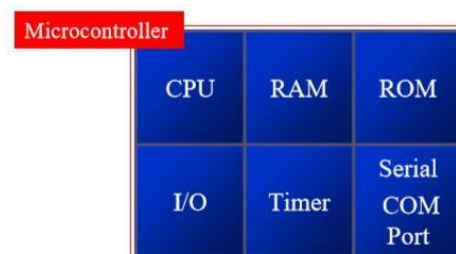
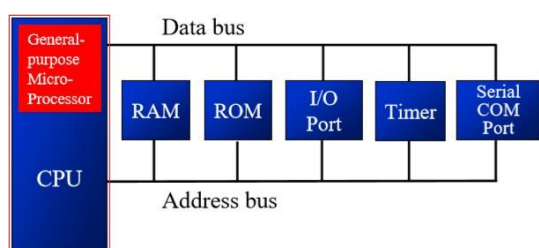


Module – 1

8051 Microcontroller

Microprocessor vs Microcontroller

- General-purpose microprocessors
 - Must add RAM, ROM, I/O ports, and timers externally to make them functional
 - Make the system bulkier and much more expensive
 - Have the advantage of versatility on the amount of RAM, ROM, and I/O ports
- Microcontroller
 - The fixed amount of on-chip ROM, RAM, and number of I/O ports makes them ideal for many applications in which cost and space are critical
 - In many applications, the space it takes, the power it consumes, and the price per unit are much more critical considerations than the computing power



Microprocessor	Microcontroller
Microprocessor contains ALU, General purpose registers, stack pointer, program counter, clock timing circuit, interrupt circuit	Microcontroller contains the circuitry of microprocessor, and in addition it has built in ROM, RAM, I/O Devices, Timers/Counters etc.
It has many instructions to move data between memory and CPU	It has few instructions to move data between memory and CPU
Few bit handling instruction	It has many bit handling instructions
Less number of pins are multifunctional	More number of pins are multifunctional
Single memory map for data and code (program)	Separate memory map for data and code (program)
Access time for memory and IO are more	Less access time for built in memory and IO.
Microprocessor based system requires additional hardware	It requires less additional hardware
More flexible in the design point of view	Less flexible since the additional circuits which is residing inside the microcontroller is fixed for a particular microcontroller
Large number of instructions with flexible addressing modes	Limited number of instructions with few addressing modes

Microcontrollers for Embedded Systems

- An embedded product uses a microprocessor (or microcontroller) to do one task and one task only
 - There is only one application software that is typically burned into ROM
- A PC, in contrast with the embedded system, can be used for any number of applications
 - It has RAM memory and an operating system that loads a variety of applications into RAM and lets the CPU run them
 - A PC contains or is connected to various embedded products
 - Each one peripheral has a microcontroller inside it that performs only one task

Criteria for Choosing a Microcontroller

- Meeting the computing needs of the task at hand efficiently and cost effectively
 - Speed
 - Packaging
 - Power consumption
 - The amount of RAM and ROM on chip
 - The number of I/O pins and the timer on chip
 - How easy to upgrade to higher performance or lower power-consumption versions
 - Cost per unit
- Availability of software development tools, such as compilers, assemblers, and debuggers
- Wide availability and reliable sources of the microcontroller
- The 8051 family has the largest number of diversified (multiple source) suppliers
 - Intel (original)
 - Atmel
 - Philips/Sigmetics
 - AMD
 - Infineon (formerly Siemens)
 - Matra
 - Dallas Semiconductor/Maxim

Harvard and Von Neumann Architectures

- **Harvard Architecture**—a type of computer architecture where the instructions (program code) and data are stored in separate memory spaces

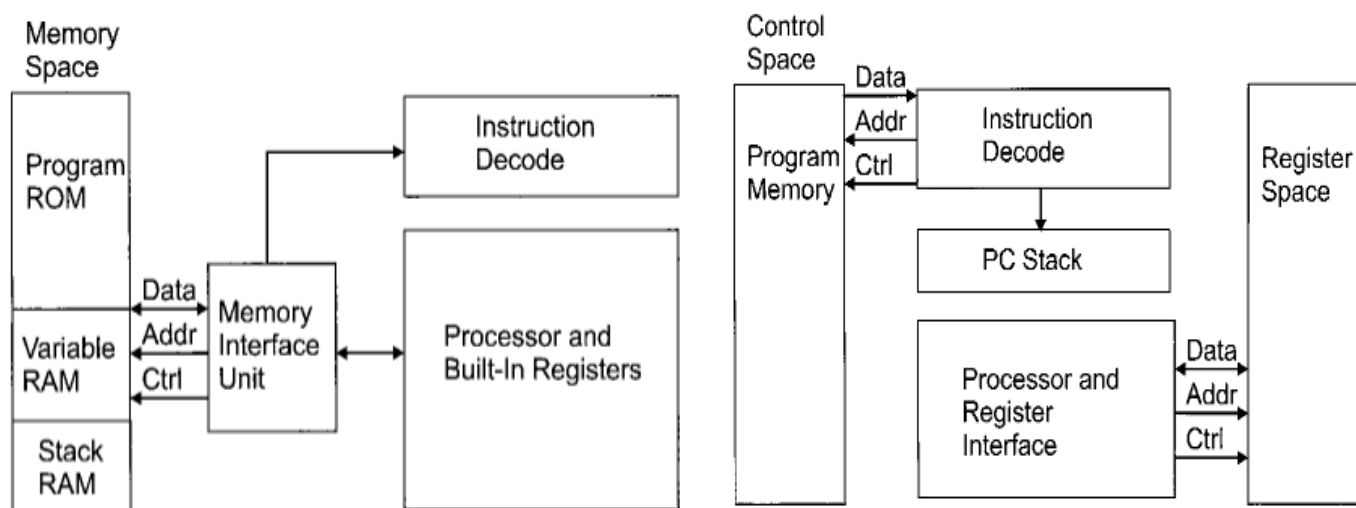
Example: Intel 8051 architecture

- **Von Neumann Architecture**—another type of computer architecture where the instructions and data are stored in the same memory space

Example: Intel x86 architecture (Intel Pentium, AMD Athlon, etc.)

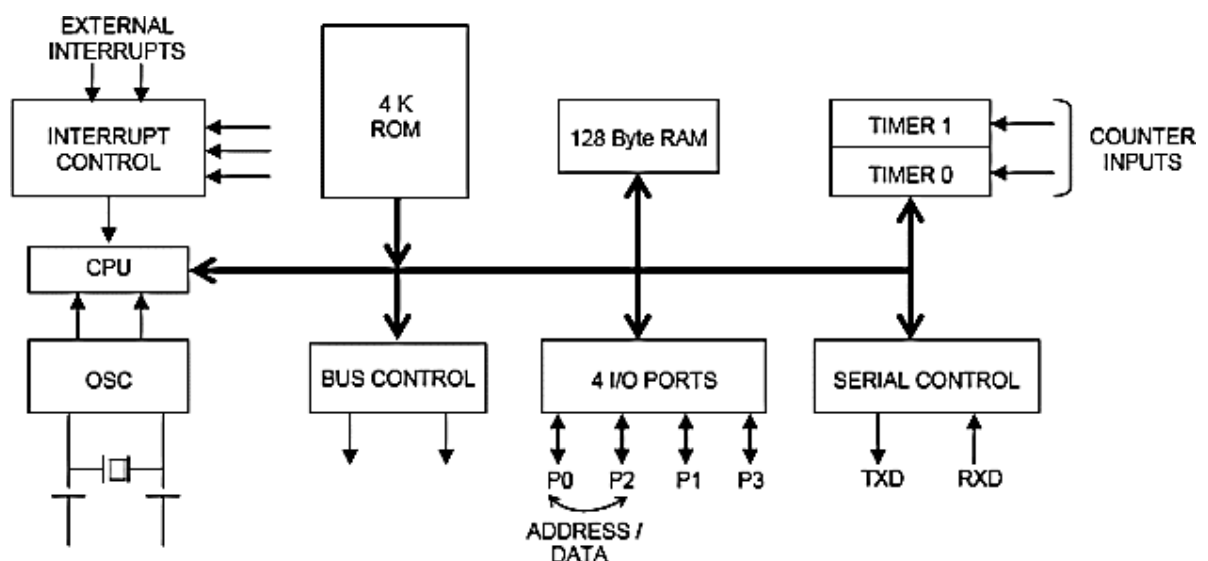
Difference between Von Neumann(Princeton) and Harvard Architecture

Von Neumann Architecture	Harvard Architecture
Based on the stored program computer concept	Harvard Mark I relay based computer system
Use common bus to transfer data and the instructions	Use separate buses to transfer data and the instruction
Use same physical memory address for instructions and the data	Use separate physical memory address for instructions and the data
Need two clock cycles to execute single instruction	Instructions are execute in single cycle no need two cycles
Cheaper to use	Costly than Von Neumann
Simple to use	More complex than Von Neumann
CPU have not access to read or write data and the instructions in a same time	CPU have access to read or write data and the instructions in a same time
Mainly use in personal computers	Mainly use in the micro controllers
Speed is limited than Harvard	Speed is high rather than von Neumann
Pipeline strategies are not possible	Pipeline strategies are possible



	RISC	CISC
Instruction Set Complexity	Supports a smaller number of instructions that perform simpler operations.	Supports a wide variety of instructions for complex operations.
Instruction Format	Uses a fixed-length instruction format.	Can have variable-length instruction formats.
Pipeline Design	Has a simpler pipeline design.	Can have longer pipelines with more complex stages.
Memory Access	Relies on load/store architecture; memory access through load and store instructions.	Supports instructions that can directly operate on memory.
Performance and Optimization	Designed for executing instructions in a small number of clock cycles.	May require more clock cycles to execute instructions
Code Density	May require more instructions to perform a task, resulting in larger program sizes.	Can often perform more operations in a single instruction, leading to smaller program sizes.

8051 Architecture



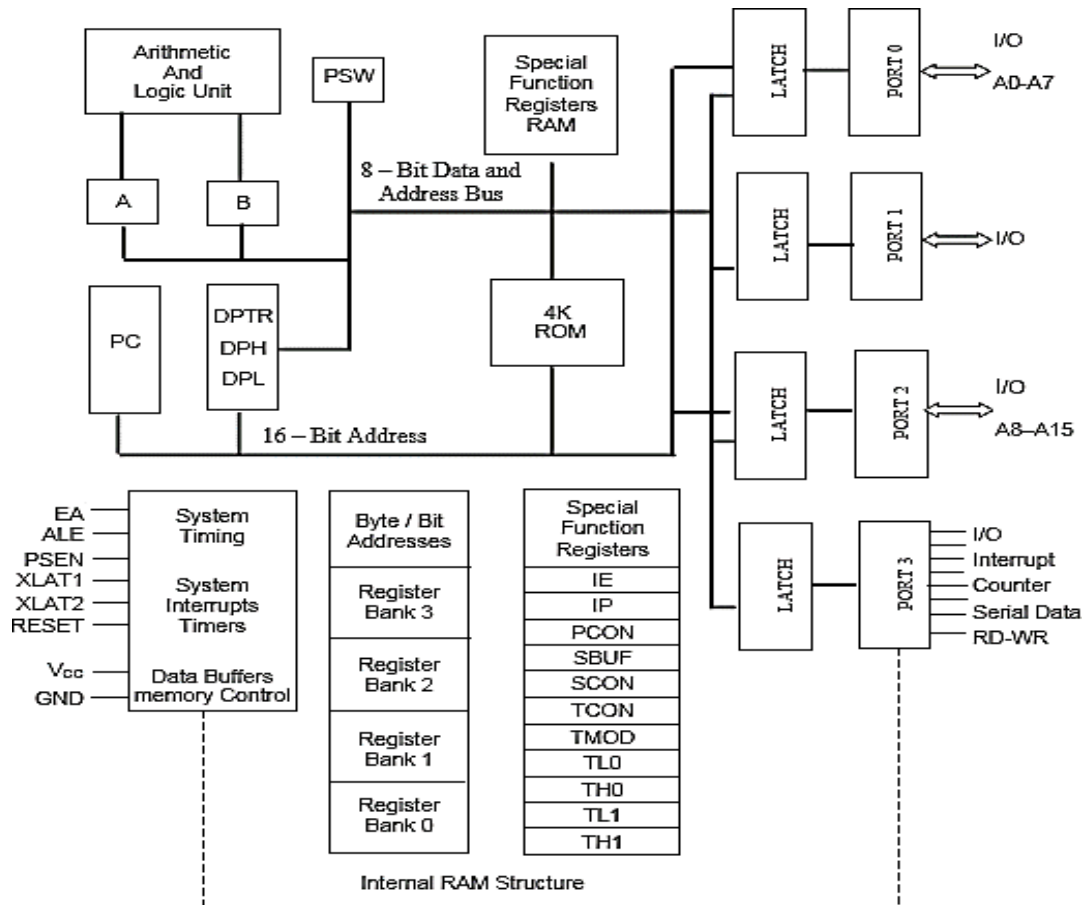
General Block Diagram of 8051 Microcontroller

Salient features of 8051 microcontroller are given below.

- Eight bit CPU
- On chip clock oscillator

- 4Kbytes of internal program memory (code memory) [ROM]
- 128 bytes of internal data memory [RAM]
- 64 Kbytes of external program memory address space.
- 64 Kbytes of external data memory address space.
- 32 bi directional I/O lines (can be used as four 8 bit ports or 32 individually addressable I/O lines)
- Two 16 Bit Timer/Counter :T0, T1
- Full Duplex serial data receiver/transmitter
- Four Register banks with 8 registers in each bank.
- Sixteen bit Program counter (PC) and a data pointer (DPTR)
- 8 Bit Program Status Word (PSW)
- 8 Bit Stack Pointer
- Five vector interrupt structure (RESET not considered as an interrupt.)
- 8051 CPU consists of 8 bit ALU with associated registers like accumulator 'A', B register, PSW, SP, 16 bit program counter, stack pointer.
- ALU can perform arithmetic and logic functions on 8 bit variables.
- 8051 has 128 bytes of internal RAM which is divided into
 - Working registers [00 – 1F]
 - Bit addressable memory area [20 – 2F]
 - General purpose memory area (Scratch pad memory) [30-7F]

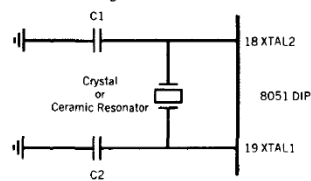
8051 Microcontroller Architecture



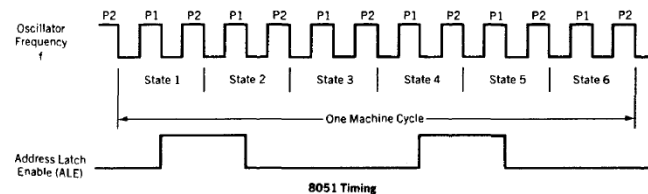
- 8051 has 4 K Bytes of internal ROM. The address space is from 0000 to 0FFFh. If the program size is more than 4 K Bytes 8051 will fetch the code automatically from external memory.
- Accumulator is an 8 bit register widely used for all arithmetic and logical operations. Accumulator is also used to transfer data between external memory. B register is used along with Accumulator for multiplication and division. A and B registers together is also called MATH registers.
- PSW (Program Status Word). This is an 8 bit register which contains the arithmetic status of ALU and the bank select bits of register banks.
- **The heart of the 8051 is the circuitry that generates the clock pulses** by which all internal operations are synchronized.
 - Pins **XTAL1** and **XTAL2** are provided for connecting a resonant network to form an oscillator.
 - The 8051 requires an **external oscillator circuit**. The oscillator circuit **usually runs around 12MHz**. the crystal generates **12M pulses in one second**. The pulse is used to **synchronize the system operation** in a controlled pace.
 - A machine cycle is **minimum amount time a simplest machine instruction** must take.
 - An **8051 machine cycle consists of 12 crystal pulses** (ticks).
 - Instruction with a memory operand needs multiple memory accesses (machine cycles).

- Typically, a quartz crystal and capacitors are employed, as shown in Figure.

Oscillator Circuit and Timing

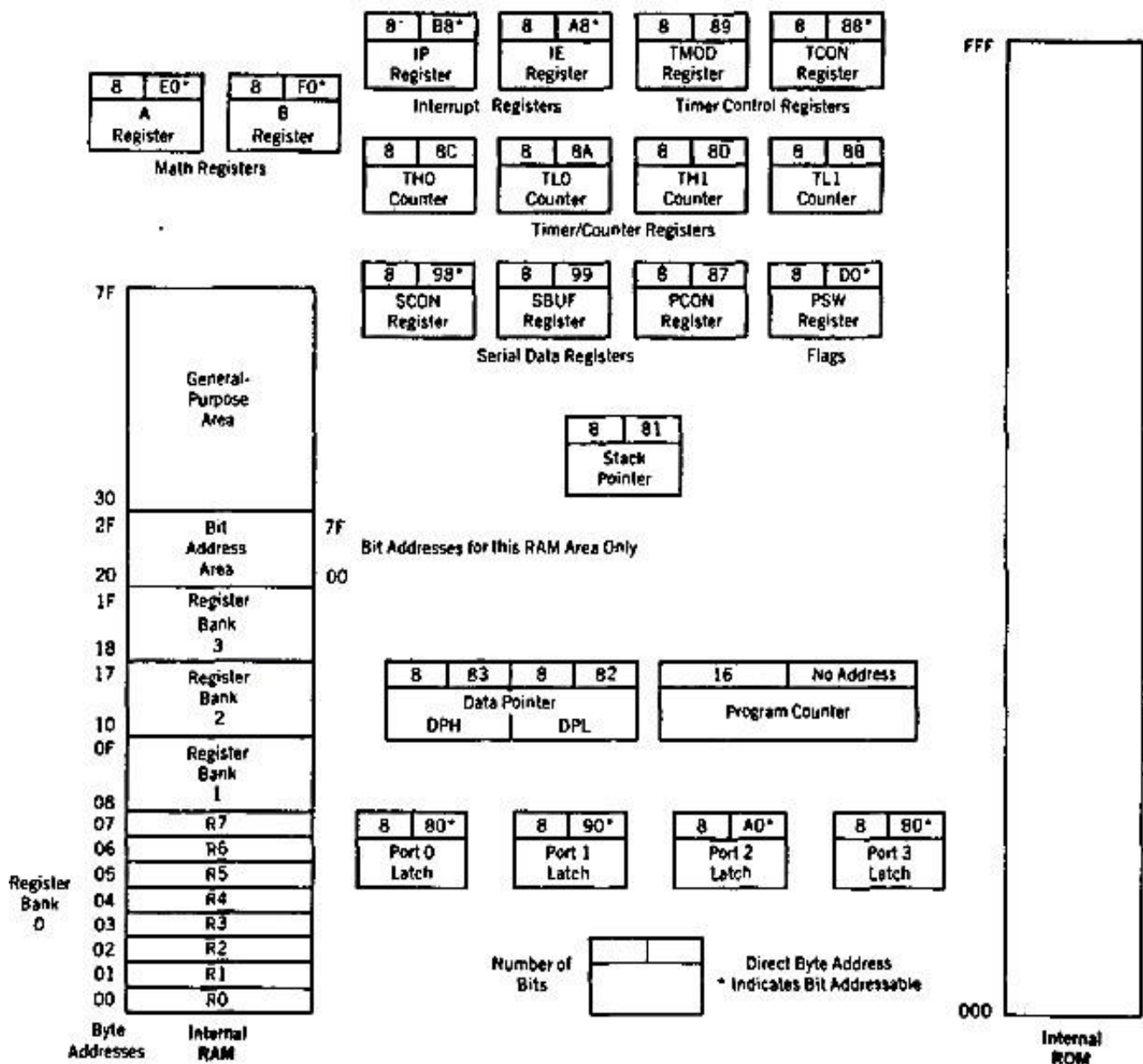


Crystal or Ceramic Resonator Oscillator Circuit



8051 Timing

8051 Programming Model



A and B CPU Registers

- The 8051 contains **34 general-purpose**, or working, registers. Two of these, registers A and B.
- The other **32 are arranged as part of internal RAM in four banks, B0-B3, of eight registers each, named R0 to R7.**
- The A (accumulator) register is **used for many operations**, including addition, subtraction, integer multiplication and division, and Boolean bit manipulations.
- The A register is also used for **all data transfers between the 8051 and any external memory.**
- The **B register is used with the A register for multiplication and division operations.**

Program Counter (PC) and Data Pointer (DPTR)

- Program instruction bytes are fetched from locations in memory that are addressed by the PC.
- The PC is **automatically incremented after every instruction byte is fetched** and may also be altered by certain instructions.
- The PC is the only register that **does not have an internal address.**
- The DPTR register is made up of two 8-bit registers, named DPH and DPL
- Are used to furnish memory addresses **for internal and external code access and external data access.**
- The DPTR is under the control of program instructions
- Can be specified by its 16-bit name, DPTR, or by each individual byte name, DPH and DPL.
- DPTR does not have a single internal address; DPH and DPL are each assigned an address.

Flags and the Program Status Word (PSW)

- Flags are 1-bit registers provided to store the results of certain program instructions.
- Other instructions can test the condition of the flags and make decisions based upon the flag states.
- The 8051 has **four math flags that respond automatically to the outcomes of math operations** and three general-purpose user flags that can be set to 1 or cleared to 0 by the programmer as desired.
- The math flags include **carry (C), auxiliary carry (AC), overflow (OY), and parity (P).**
- User flags are named **FO, GFO, and GFI**; they are general-purpose flags.
- Note that all of the flags can be set and cleared by the programmer.

7	6	5	4	3	2	1	0
CY	AC	F0	RS1	RS0	OV	-	P

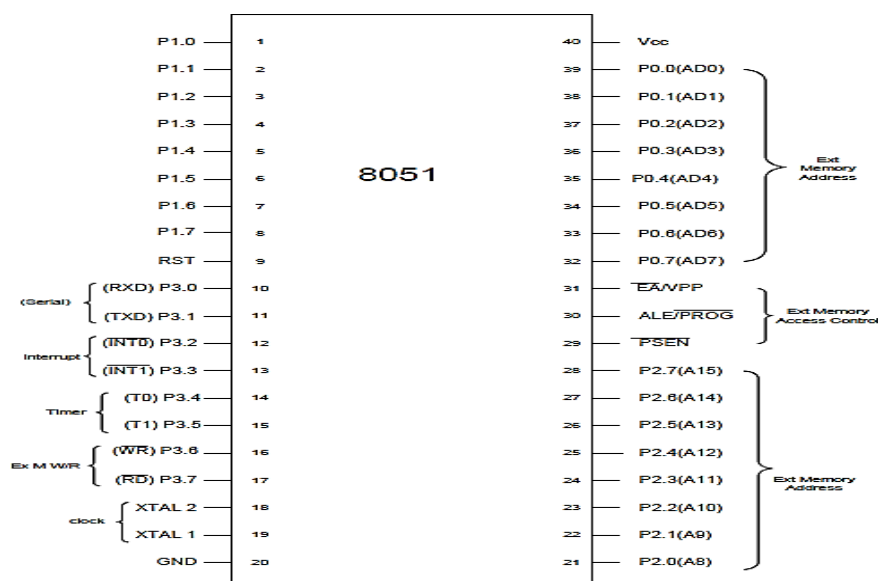
Special Function Registers

- The 8051 has a group of specific internal registers, each called a **special-function register (SFR)**, which may be addressed much like internal RAM, using addresses from **80h to FFh**.
- Some SFRs** (marked with an asterisk*) are also **bit addressable**; this feature **allows the programmer to change only what needs to be altered**, leaving the remaining bits in that SFR unchanged.
- Not all of the addresses from 80h to FFh are used for SFRs**, and attempting to use an address that is not defined, or "empty" results in unpredictable results.
- SFRs are named in certain opcodes by their functional names, such as A or TH0, and are referenced by other opcodes by their addresses, such as 0E0h or 8Ch.
- Note that *any* address used in the program *must* start with a number; thus address E0h for the A SFR begins with 0.
- Failure to use this number convention will result in an assembler error when the program is assembled.

NAME	FUNCTION	INTERNAL RAM ADDRESS (HEX)
A	Accumulator	0E0
B	Arithmetic	0F0
DPH	Addressing external memory	83
DPL	Addressing external memory	82
IE	Interrupt enable control	0A8
IP	Interrupt priority	0B8
P0	Input/output port latch	80
P1	Input/output port latch	90
P2	Input/output port latch	A0
P3	Input/output port latch	0B0

NAME	FUNCTION	INTERNAL RAM ADDRESS (HEX)
PCON	Power control	87
PSW	Program status word	0D0
SCON	Serial port control	98
SBUF	Serial port data buffer	99
SP	Stack pointer	81
TMOD	Timer/counter mode control	89
TCON	Timer/counter control	88
TL0	Timer 0 low byte	8A
TH0	Timer 0 high byte	8C
TL1	Timer 1 low byte	8B
TH1	Timer 1 high byte	8D

Pin Diagram

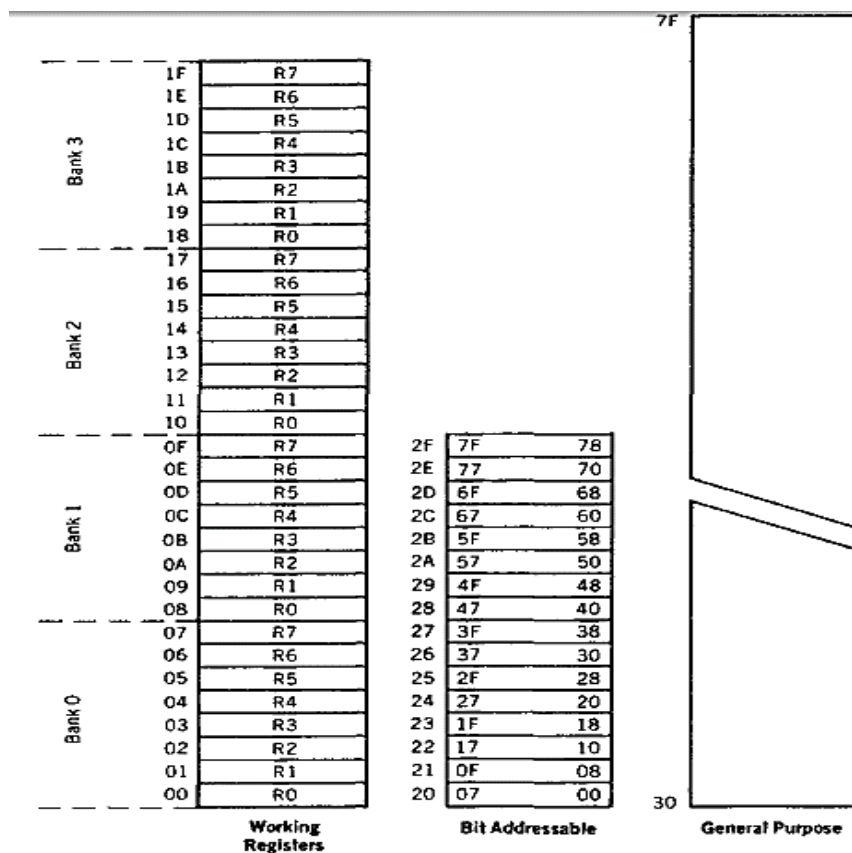


Pinout Description

Pins 1-8	PORT 1. Each of these pins can be configured as an input or an output.
Pin 9	RESET. A logic one on this pin disables the microcontroller and clears the contents of most registers. In other words, the positive voltage on this pin resets the microcontroller. By applying logic zero to this pin, the program starts execution from the beginning.
Pins 10-17	PORT 3. Similar to port 1, each of these pins can serve as general input or output. Besides, all of them have alternative functions
Pin 10	RXD. Serial asynchronous communication input or Serial synchronous communication output.
Pin 11	TXD. Serial asynchronous communication output or Serial synchronous communication clock output.
Pin 12	INT0. External Interrupt 0 input
Pin 13	INT1. External Interrupt 1 input
Pin 14	T0. Counter 0 clock input
Pin 15	T1. Counter 1 clock input
Pin 16	WR. Write to external (additional) RAM
Pin 17	RD. Read from external RAM
Pin 18, 19	XTAL2, XTAL1. Internal oscillator input and output. A quartz crystal which specifies operating frequency is usually connected to these pins.
Pin 20	GND. Ground.
Pin 21-28	Port 2. If there is no intention to use external memory then these port pins are configured as general inputs/outputs. In case external memory is used, the higher address byte, i.e. addresses A8-A15 will appear on this port. Even though memory with capacity of 64Kb is not used, which means that not all eight port bits are used for its addressing, the rest of them are not available as inputs/outputs.
Pin 29	PSEN. If external ROM is used for storing program then a logic zero (0) appears on it every time the microcontroller reads a byte from memory.
Pin 30	ALE. Prior to reading from external memory, the microcontroller puts the lower address byte (A0-A7) on P0 and activates the ALE output. After receiving signal from the ALE pin, the external latch latches the state of P0 and uses it as a memory chip address. Immediately after that, the ALE pin is returned its previous logic state and P0 is now used as a Data Bus.
Pin 31	EA. By applying logic zero to this pin, P2 and P3 are used for data and address transmission with no regard to whether there is internal memory or not. It means that even there is a program written to the microcontroller, it will not be executed. Instead, the program written to external ROM will be executed. By applying logic one to the EA pin, the microcontroller will use both memories, first internal then external (if exists).
Pin 32-39	PORT 0. Similar to P2, if external memory is not used, these pins can be used as general inputs/outputs. Otherwise, P0 is configured as address output (A0-A7) when the ALE pin is driven high (1) or as data output (Data Bus) when the ALE pin is driven low (0).
Pin 40	VCC. +5V power supply.

Internal Memory organization

- A functioning computer **must have**
 - **MEMORY FOR PROGRAM CODE BYTES, COMMONLY IN ROM**
 - **RAM MEMORY FOR VARIABLE DATA THAT CAN BE ALTERED AS THE PROGRAM RUNS.**
- Additional memory can be added externally using suitable circuits.
- 8051 has a **Harvard architecture**, which uses the *same address*, in *different memories*, for code and data.
 - Internal circuitry accesses the correct memory based upon the nature of the operation in progress.



Internal RAM

- Thirty-two bytes from address **00h to 1Fh** that **make up 32 working registers** organized as four banks of eight registers each. (Bank0- Bank3; with each bank having registers R0-R7)
- Each register can be **addressed by name** (when its bank is selected) **or by its RAM address**.
- Thus R0 of bank 3 is R0 (if bank 3 is currently selected) or address 18h (whether bank 3 is selected or not).
- Bits **RS0** and **RS1** in the **PSW** **determine** which bank of registers is currently in use.
- **Register banks not selected can be used as general-purpose RAM.**

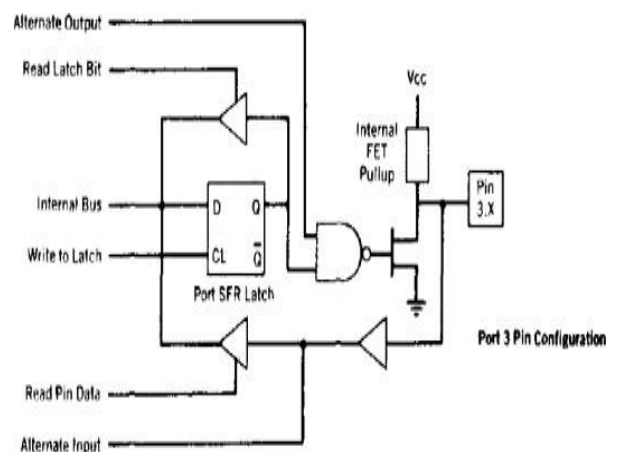
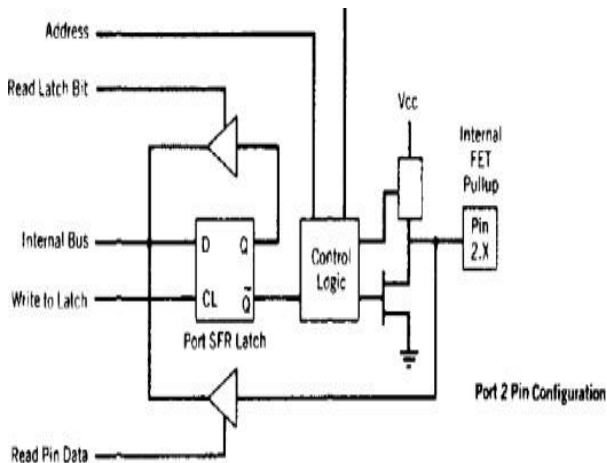
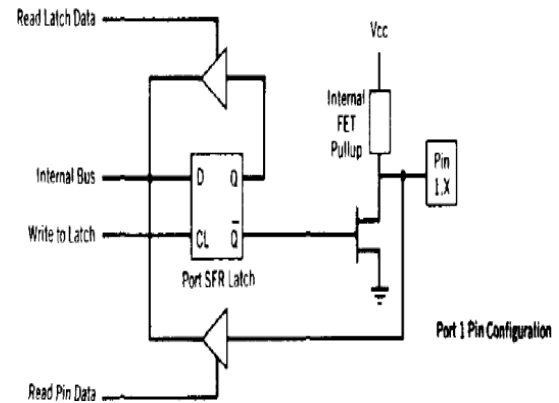
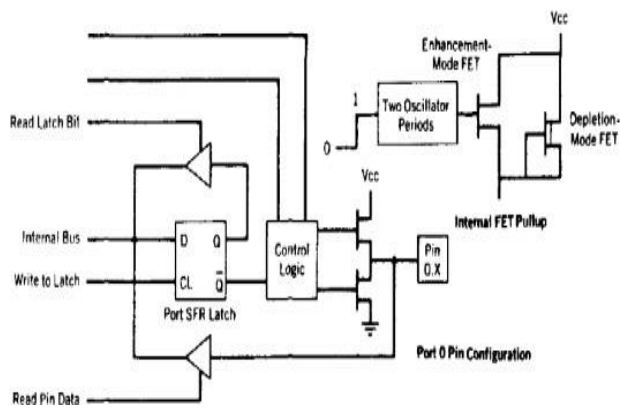
- **Bank 0 is selected upon reset.**
- A **bit-addressable** area of 16 bytes occupies RAM **byte addresses 20h to 2Fh**, forming a **total of 128 addressable bits**.
- An addressable bit may be specified by its **bit address of 00h to 7Fh**, or 8 bits may form any **byte address from 20h to 2Fh**.
 - Thus, for example, bit address 4Fh is also bit 7 of byte address 29h.
 - Addressable bits are useful when the program need only remember a binary event (switch on, light off, etc.).
- A **general-purpose** RAM area above the bit area, **from 30h to 7Fh**, addressable as bytes.

Internal ROM

- The 8051 is organized so that data memory and program code memory can be in **two entirely different physical memory entities; each has the same address ranges**.
- A corresponding block of internal program code, contained in an internal ROM, occupies code address space 0000h to 0FFFh.
- The PC is ordinarily used to address program code bytes from addresses 0000h to 0FFFh.
- Program addresses **higher than 0FFFh**, which exceed the internal ROM capacity, will cause the 8051 to **automatically fetch code bytes from external program memory**.
- **Code bytes can also be fetched exclusively from an external memory**, addresses 0000h to FFFFh, by connecting the external access pin (EA pin 31 on the DIP) to **ground**.
- **The PC does not care where the code is**; the circuit designer decides whether the code is found totally in internal ROM, totally in external ROM, or in a combination of internal and external ROM.

Input/ Output Pins, Ports, and Circuits

- Ports can be accessed directly by instructions during program execution
- I/O ports are memory mapped, they are treated as memory locations
- All ports are bit addressable
- Each PIN consists of a D latch, I/P buffer and O/P driver
- SFRs for each port is made of 8-latches
- Accessed by SFRs address or name of that port
- The four 8-bit I/O ports P0, P1, P2 and P3 each uses 8 pins
- All the ports upon RESET are configured as output, ready to be used as output ports
 - When the first 0 is written to a port, it becomes an output
 - To reconfigure it as an input, a 1 must be sent to the port
 - To use any of these ports as an input port, it must be programmed



External Memory (ROM & RAM) interfacing

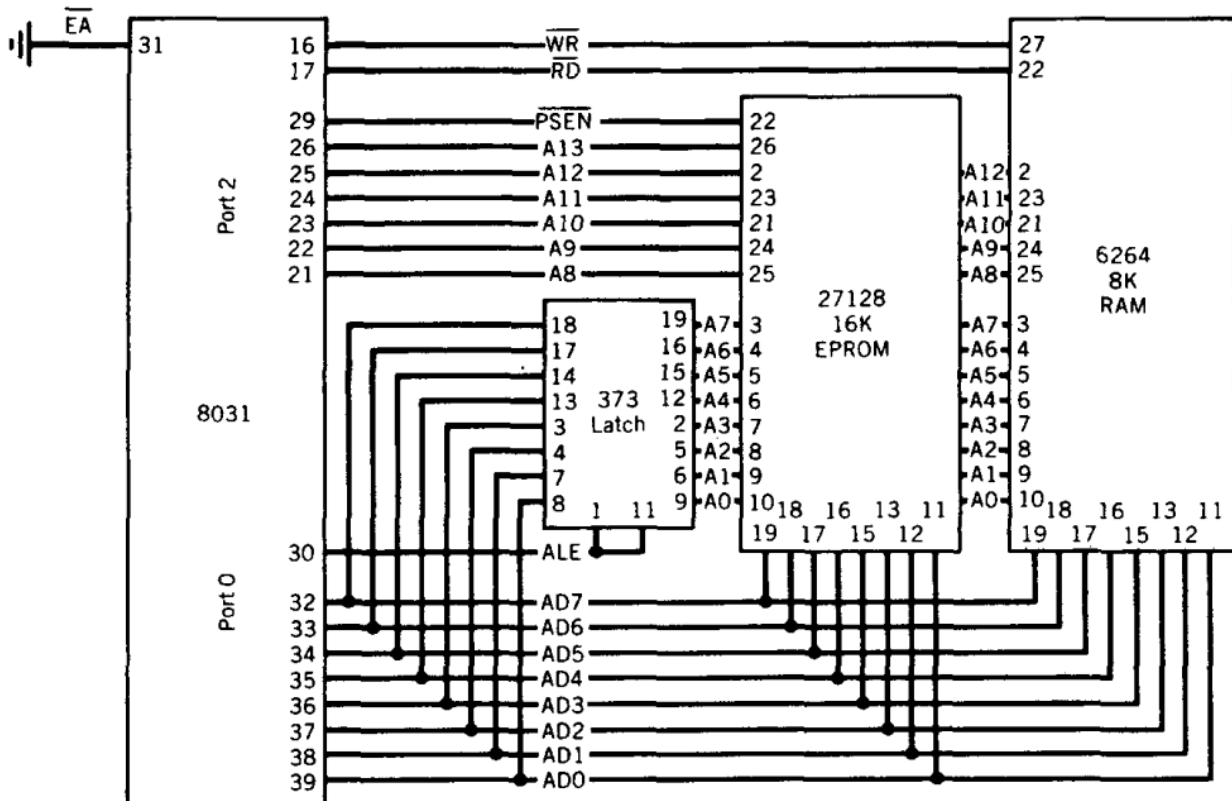
Eg. Interfacing of 16 K Byte of RAM and 32 K Byte of EPROM to 8051

Number of address lines required for 16 Kbyte memory is 14 lines and that of 32Kbytes of memory is 15 lines.

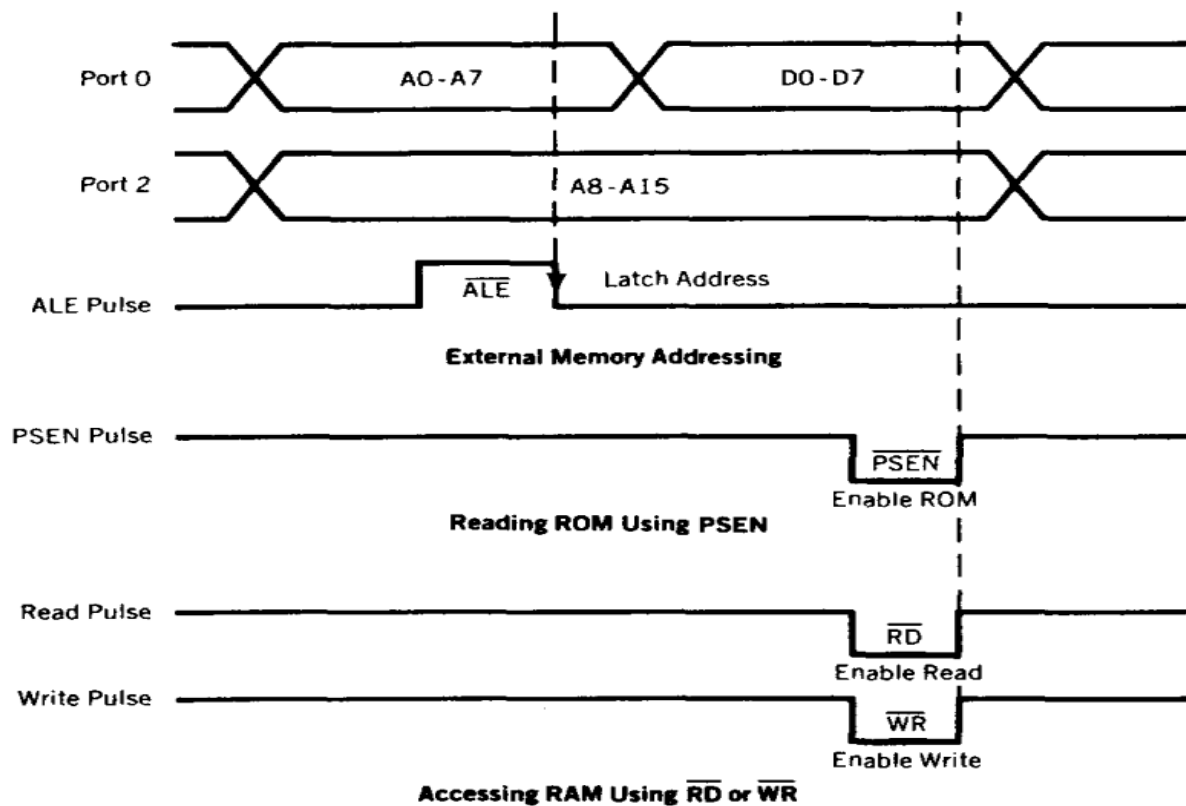
The connections of external memory is shown below.

The lower order address and data bus are multiplexed. De-multiplexing is done by the latch. Initially the address will appear in the bus and this latched at the output of latch using ALE signal. The output of the latch is directly connected to the lower byte address lines of the memory. Later data will be available in this bus. Still the latch output is address itself. The higher byte of address bus is directly connected to the memory. The number of lines connected depends on the memory size.

External Memory Connections



External Memory Timing



The RD and WR (both active low) signals are connected to RAM for reading and writing the data.

PSEN of microcontroller is connected to the output enable of the ROM to read the data from the memory.

EA (active low) pin is always grounded if we use only external memory. Otherwise, once the program size exceeds internal memory the microcontroller will automatically switch to external memory.

- The number of bits that a semiconductor memory chip can store is called **chip capacity**
 - It can be in units of Kbits (kilobits), Mbits (megabits), and so on.
- Memory chips are organized into a number of locations within the IC.
 - Each location can hold 1 bit, 4 bits, 8 bits, or even 16 bits, depending on how it is designed internally
 - The number of locations within a memory IC depends on the address pins
 - The number of bits that each location can hold is always equal to the number of data pins
- A memory chip contains 2^x locations, where x is the number of address pins.
- Each location contains y bits, where y is the number of data pins on the chip.
- The entire chip will contain $2^x \times y$ bits

Example 1.1

A given memory chip has 12 address pins and 4 data pins. Find:

(a) The organization, and (b) the capacity.

Solution:

- a) This memory chip has **4096 locations ($2^{12} = 4096$)**, and each location **can hold 4 bits** of data. This gives an organization of **4096×4** , often represented as **$4K \times 4$** .
- b) The **capacity is equal to 16K** bits since there is a total of 4K locations and each location can hold 4 bits of data.

Example 1.2

A 512K memory chip has 8 pins for data. Find:

(a) The organization, and (b) the number of address pins for this memory chip.

Solution:

- a) A memory chip with 8 data pins means that each location within the chip can hold 8 bits of data. To find the number of locations within this memory chip, divide the capacity by the number of data pins. $512K/8 = 64K$; therefore, the organization for this memory chip is $64K \times 8$
- b) The chip has 16 address lines since $2^{16} = 64K$