BBEE 203

Module 2

Transistor

By

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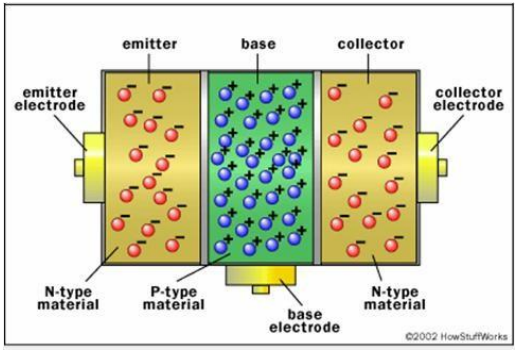
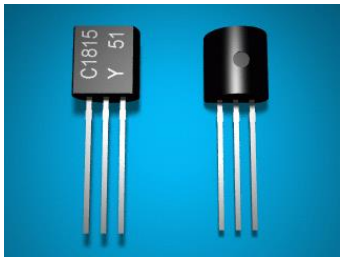
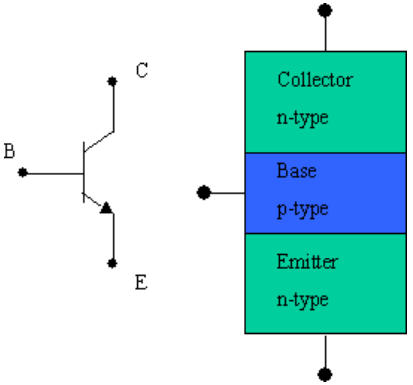
ATMECE

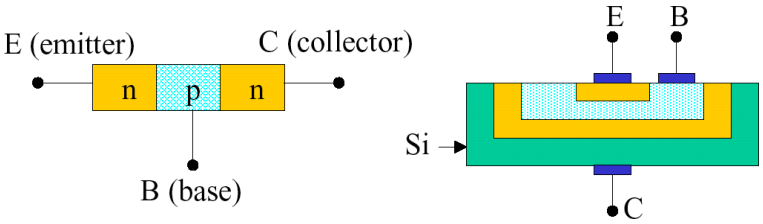




Transistors



Bardeen, Brattain and Shockley, while at Bell Laboratories, invented it in 1948 as part of a post-war effort to replace vacuum tubes with solid-state devices.



Why so called?

=> Transfer of Resistance

Transistor Types

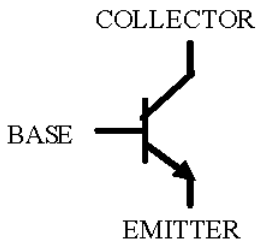
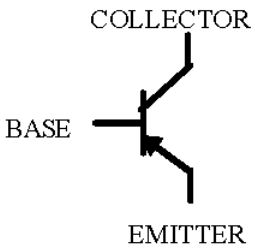
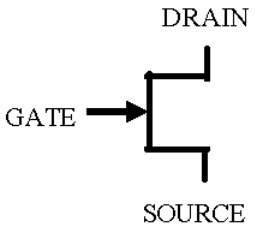
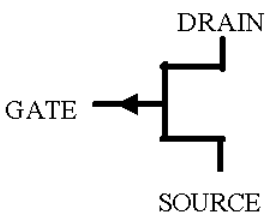
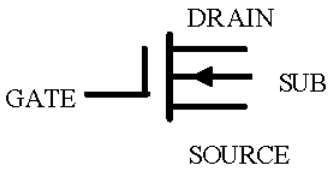
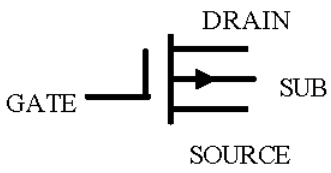
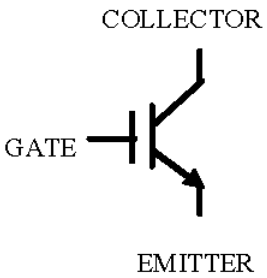
Introduction

There are three main classifications of transistors each with its own symbols, characteristics, design parameters, and applications. See below and the following pages for additional details and applications on each of these transistor types. Several special-function transistor types also exist which do not fall into the categories below, such as the unijunction (UJT) transistor that is used for SCR firing and time delay applications. These special-function devices are described separately.

- Bipolar transistors are considered *current driven* devices and have a relatively low input impedance. They are available as NPN or PNP types. The designation describes the polarity of the semiconductor material used to fabricate the transistor.

- Field Effect Transistors, FET's, are referred to as *voltage driven* devices which have a high input impedance. Field Effect Transistors are further subdivided into two classifications: 1) Junction Field Effect Transistors, or JFET's, and 2) Metal Oxide Semiconductor Field Effect Transistors or MOSFET's.

- Insulated Gate Bipolar Transistors, known as IGBT's, are the most recent transistor development. This hybrid device combines characteristics of both the Bipolar Transistor with the capacitive coupled, high impedance input, of the MOS device.

DEVICE NAME	SYMBOL		CHARACTERISTICS And Applications
	NPN	PNP	
Bipolar Transistor			A small input *current* signal flowing emitter-to-base in the transistor controls the transistor emitter-to-collector internal resistance. Used as amplifiers or switches in a wide variety of equipment ranging from small signal applications to high power output devices.
FET Junction Field Effect Transistor	**N-CHANNEL** 	**P-CHANNEL** 	Input *voltage* signal is applied to the gate-source junction in a reverse biased mode, resulting in a high input impedance. Input signal varies the source-to-drain internal resistance. Applications include high input impedance amplifier circuitry.
MOS Metal Oxide Semiconductor Field Effect Transistor	**N-CHANNEL** 	**P-CHANNEL** 	Similar to the JFET above except the input *voltage* is capacitive coupled to the transistor. The device is easily fabricated, inexpensive, and has a low power drain, but is easily damaged by static discharge. Computer chips utilize CMOS
IGBT Insulated Gate Bipolar Transistor			Similar to the Bipolar NPN above except the input *voltage* is capacitive coupled to the transistor as with the MOSFET devices. Main application is as a switch for the output section of small and medium size Variable Frequency Drives (VFD's).

Bipolar Junction Transistor

Definition ;Why so called?

Bipolar transistors are called *bi*polar because the main flow of electrons through them takes place in *two* types of semiconductor material: P and N, as the main current goes from emitter to collector (or vice versa). In other words, two types of charge carriers -- electrons and holes -- comprise this main current through the transistor.

A Bipolar Junction Transistor is a Current In/Current Out Device

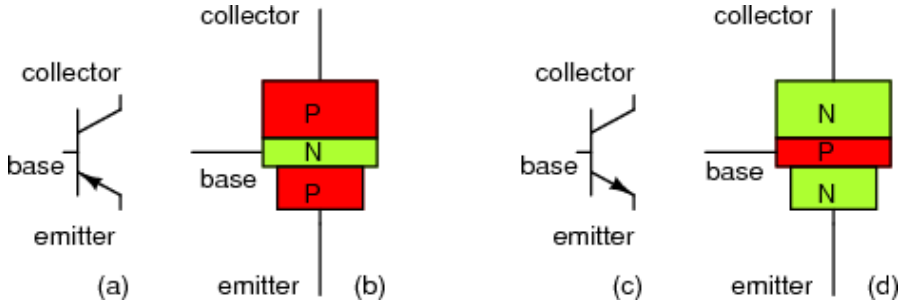
- **A Transistor can be thought of as a device that is active in only One Direction:**
- **It can draw more or less current through its load resistor.**
- **It can either Sink Current or it can Source Current, it <u>Cannot do Both.</u>**

Bipolar Junction Transistor Construction

A bipolar transistor consists of a three-layer "sandwich" of doped (extrinsic) semiconductor materials, either P-N-P in Figure below (b) or N-P-N at (d).
Each layer forming the transistor has a specific name, and each layer is provided with a wire contact for connection to a circuit. The schematic symbols are shown in Figure below (a) and (c).

Construction

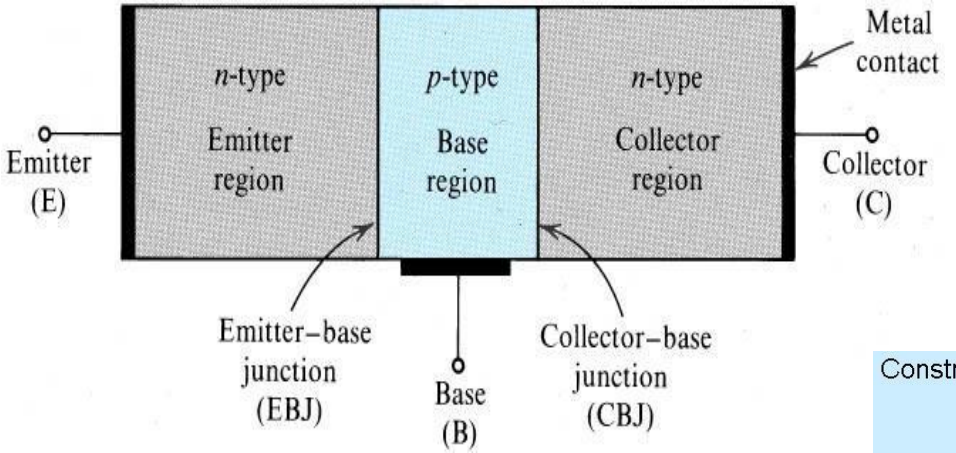
- The bipolar transistor is a three-layer semiconductor**device.**
- The base lead connects to the center semiconductor material of this three-layer device. The base region is dimensionally thin compared to the emitter and collector regions.
- Two PN (diode) junctions exist within a bipolar transistor. One PN junction exists between the emitter and the base region, a second exists between the collector and the base region. (See How to Test a Bipolar Transistor on Sheet 4.)

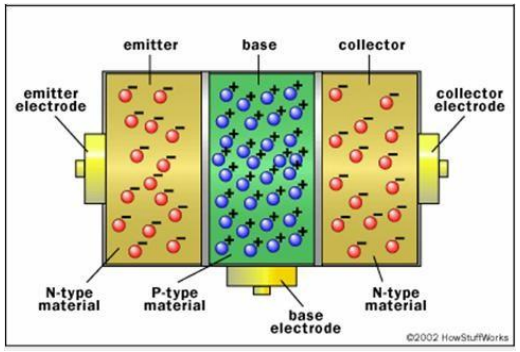


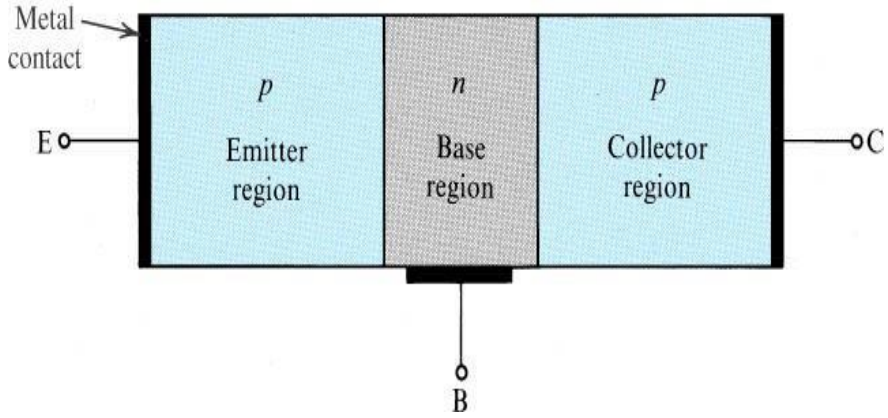
BJT transistor: (a) PNP schematic symbol, (b) construction (c) NPN symbol, (d) construction.

- The three leads or connecting terminals of a bipolar transistor are called the *Emitter*, *Base*, and *Collector*.
- Transistors function as current regulators by allowing a small current to *control* a larger current.
- The amount of current allowed between collector and emitter is primarily determined by the amount of current moving between base and emitter.

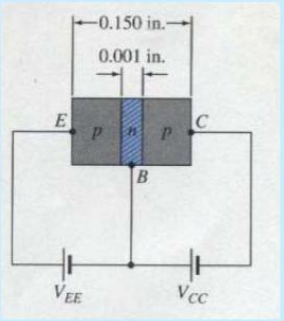
- **Emitter is heavily doped and has a moderate area as it has to provide the charge carriers for current conduction.**
- **Base is thin and very lightly doped to avoid recombination of charge carriers entering it from the emitter section.**
- **Collector is moderately doped as it has to help in providing the output current and has a large area so as to dissipate the heat developed due to the flow of a sufficiently large current.**



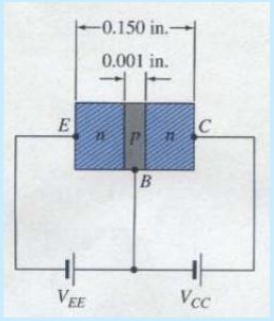




Construction of BJTs



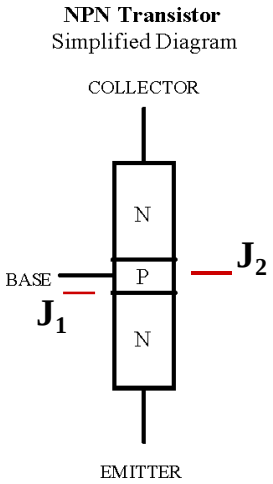
(a) pnp type and dc biasing

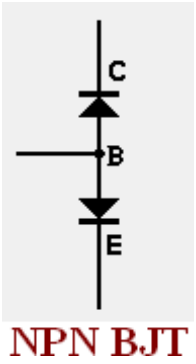


(b) npn type and dc biasing

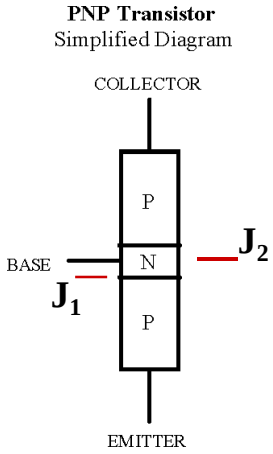
(i) Consists of three layers.
(ii) Dc biasing is necessary to establish proper region of operation for ac amplification.
(iii) The emitter layer is heavily doped, the base lightly doped and the collector only lightly doped.
(iv) The outer layers have widths much greater than the sandwiched p or n type material.
(v) E stands for Emitter, B for Base and C for Collector.
(vi) The terms bipolar reflects the fact that holes and electrons participate in the injection process into the oppositely polarized material. (Unipolar: one carrier is employed (electron or hole , ex: diode)

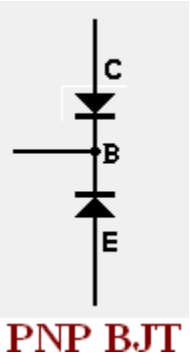
Thus, a BJT can be considered to be two PN-junctions or diodes connected back-to-back.





NPN BJT





PNP BJT

Transistor Biasing:

- **For proper BJT operation the two junctions or diodes must be biased appropriately depending upon the transistor application.**

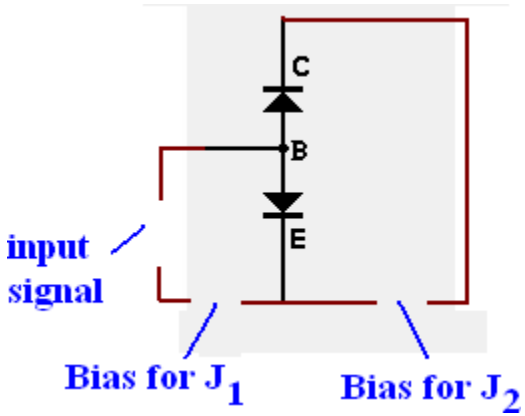
(It is necessary to bias that is apply power supply or external potential to overcome the barrier voltage) which is V_B=0.7V for Si and V_B=0.3V for Ge BJT.

- **Bias is to be applied across (1) the E-B jn or input junction (2) the C-B jn or output junction**
- **The two junctions are biased (according to BJT application) in a way that the junctions are either:**

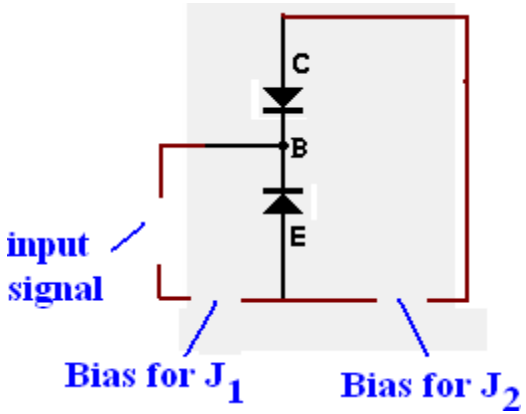
(1) forward biased and /or (2) reverse biased.

Biasing Arrangements according to BJT applications:

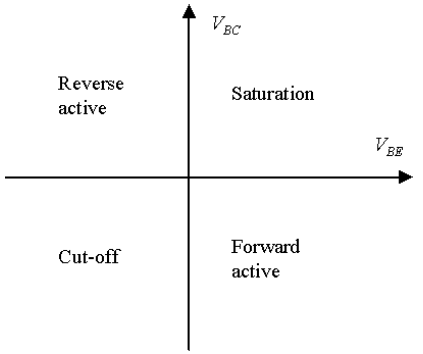
BJT Applications	Emitter-Base jn (input jn J_1)	Collector-Emitter jn (output jn J_2)	BJT Operating Mode/region
OFF-Switch	Reverse-Biased	Reverse-Biased	Cut-OFF (Input current I_B=0, Output Current I_C=0)
ON-Switch	Forward-Biased	Forward-Biased	Saturation (Input current I_B flows, Output Current I_C =maxm value)
Amplifier	Forward-Biased	Reverse-Biased	Active (Input current I_B flows, Output Current I_C flows proportional to input current)



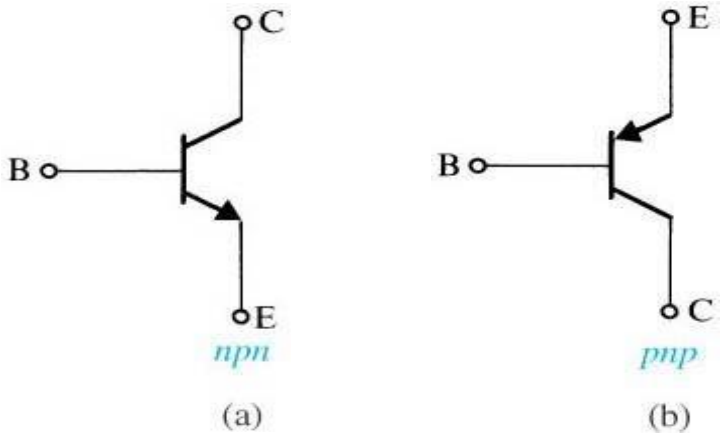
NPN BJT



PNP BJT



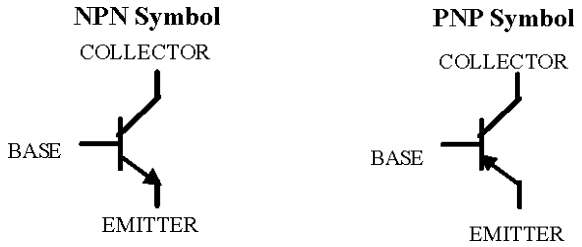
Circuit Symbols for BJTs



The emitter is distinguished by the arrowhead.

Bipolar Transistor Symbols

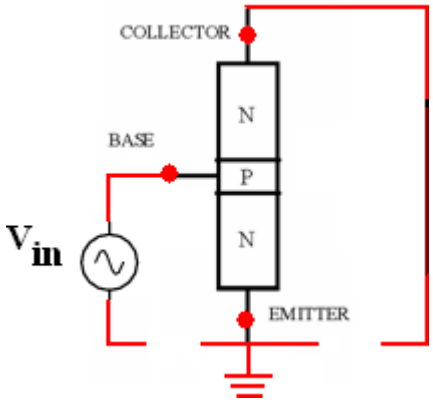
- The arrow is always on the emitter lead and points in the direction of *conventional* current flow (positive-to-negative). As with the diode, the nose of the arrow points to the negative, or N-Type semiconductor material, and the tail of the arrow is toward the P-Type material.
- The arrow on the NPN points away from the base. (Remember as NPN = Not Pointing iN.)
- The arrow on the PNP points toward the base. (Remember as PNP = Pointing iN Pointer.)

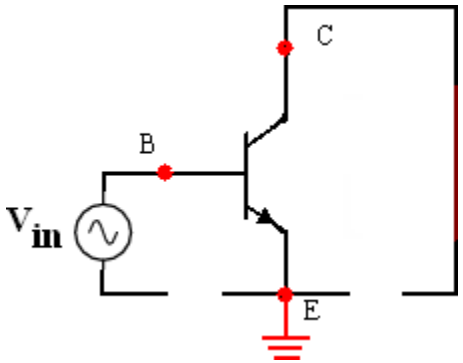


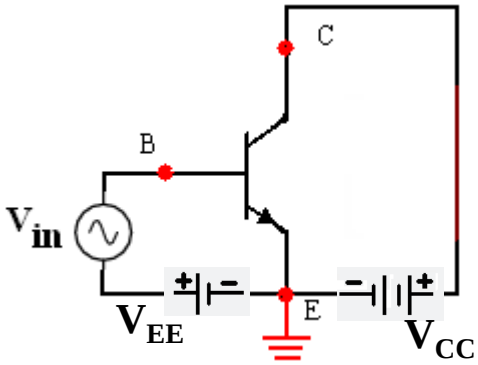
Arrows indicate the direction of conventional current flow.

Conventional current direction is the same as direction of hole flow but opposite to the direction of electron flow.

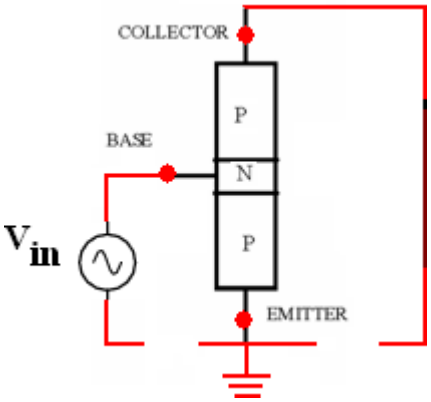
Draw the diagrams of various Biasing arrangements:

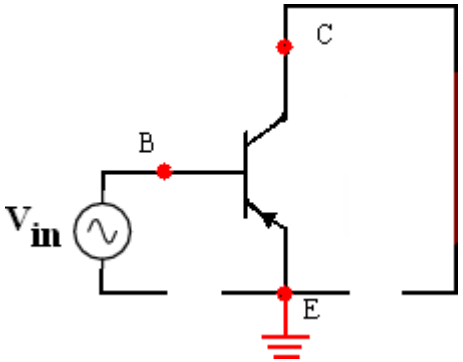


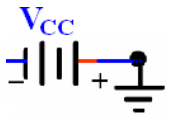


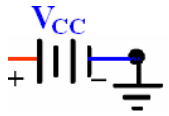


NPN BJT biased in Active mode





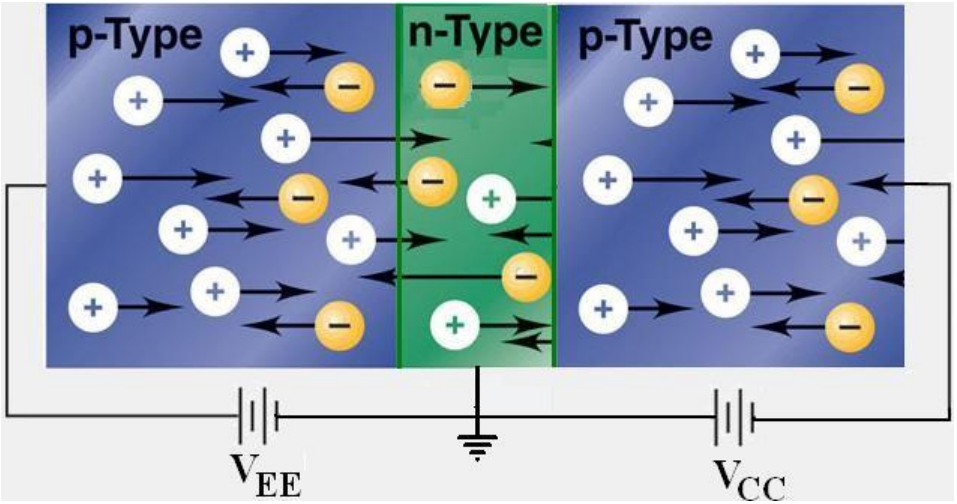




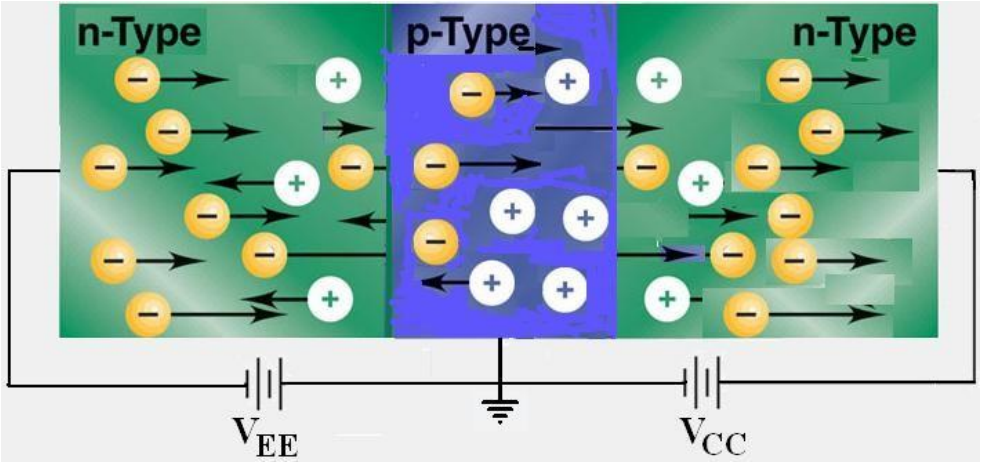
I_E

V_{EB} =0.7V

Working or Operation of an NPN BJT

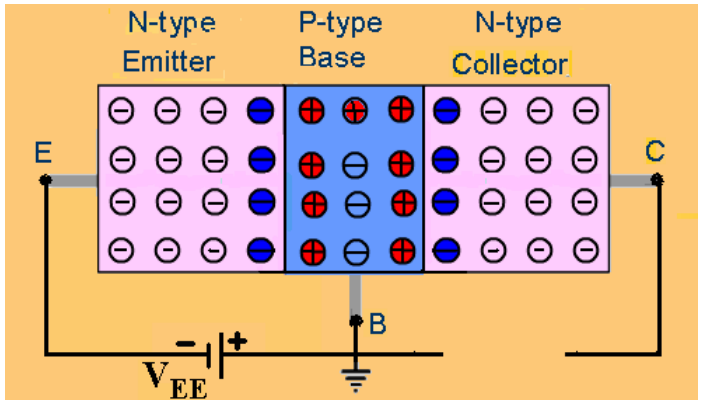


Working or Operation of an PNP BJT

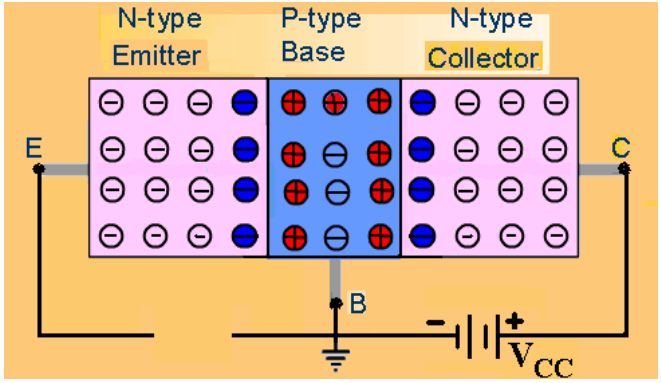


Working or Operation of an NPN BJT

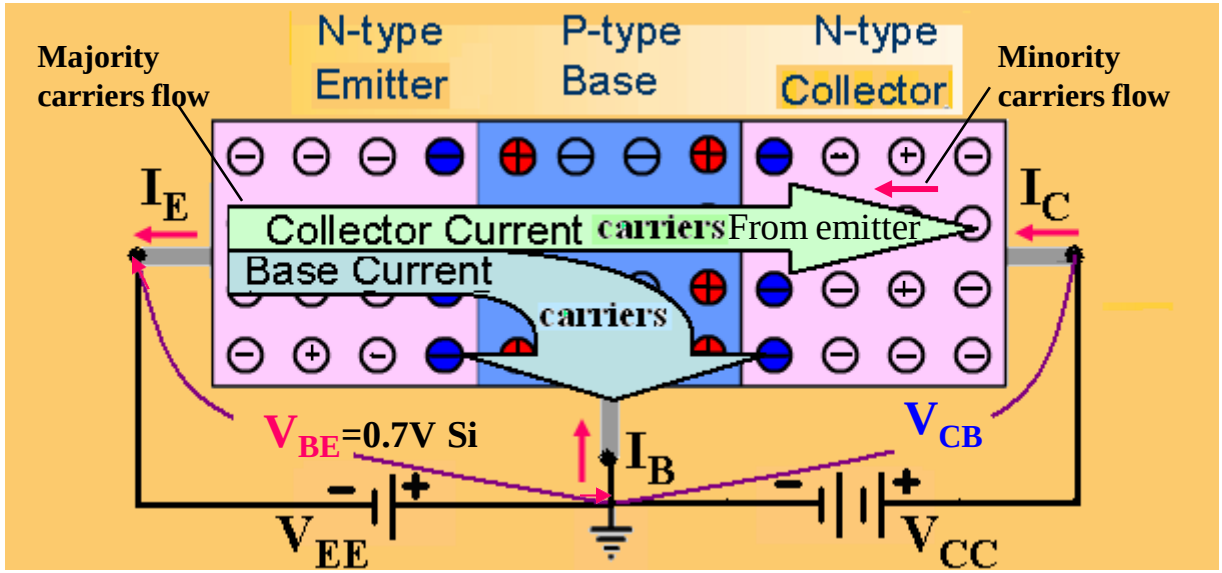
For a BJT (NPN or PNP) to function or operate or work properly the two diodes constituting the BJT must be biased appropriately. To understand the operation or working of a BJT it is always studied in the forward-active mode or as an Amplifier and hence biased accordingly.



→ Input diode F.B

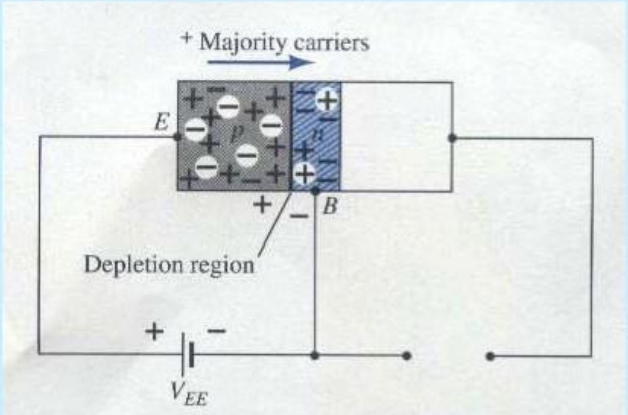


→ Output diode R.B.



NPN BJT biased to work as an Amplifier in Forward-Active mode.

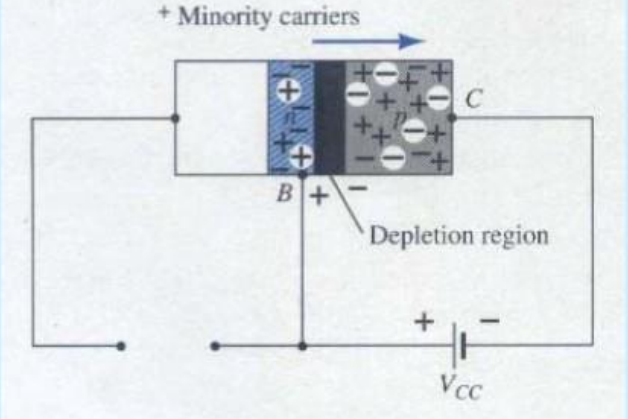
Operation of BJTs



Forward biased junction of a pnp transistor

The pnp transistor shown in this figure has been redrawn without the base-to-collector bias.

In this figure, the emitter-to-base is in the situation of forward-biased.
(p type is connected to +ve voltage terminal)
(n type is connected to –ve voltage terminal)
Here, the depletion region has been reduced in width due to the applied bias, resulting in a heavy flow of majority carriers from the p- to the n-type material.



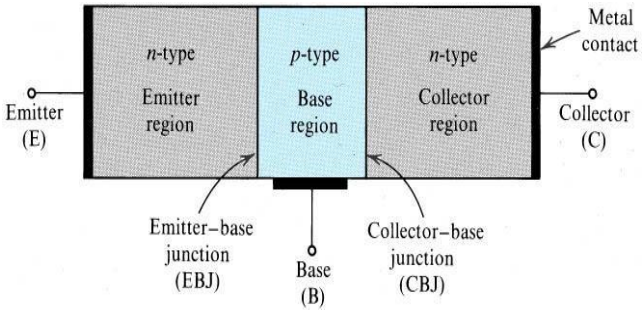
Reversed biased junction of a pnp transistor

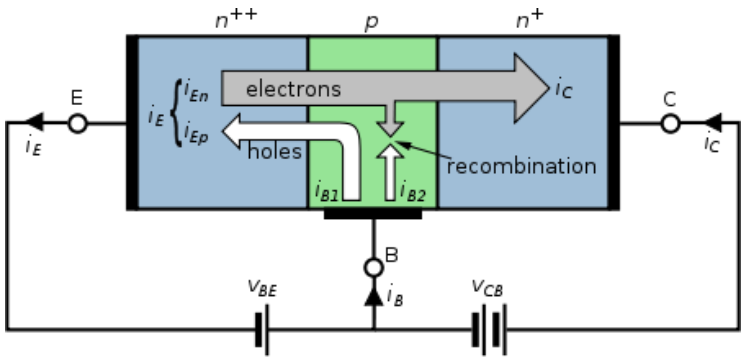
The pnp transistor shown in this figure has been redrawn without the emitter-to-base bias.

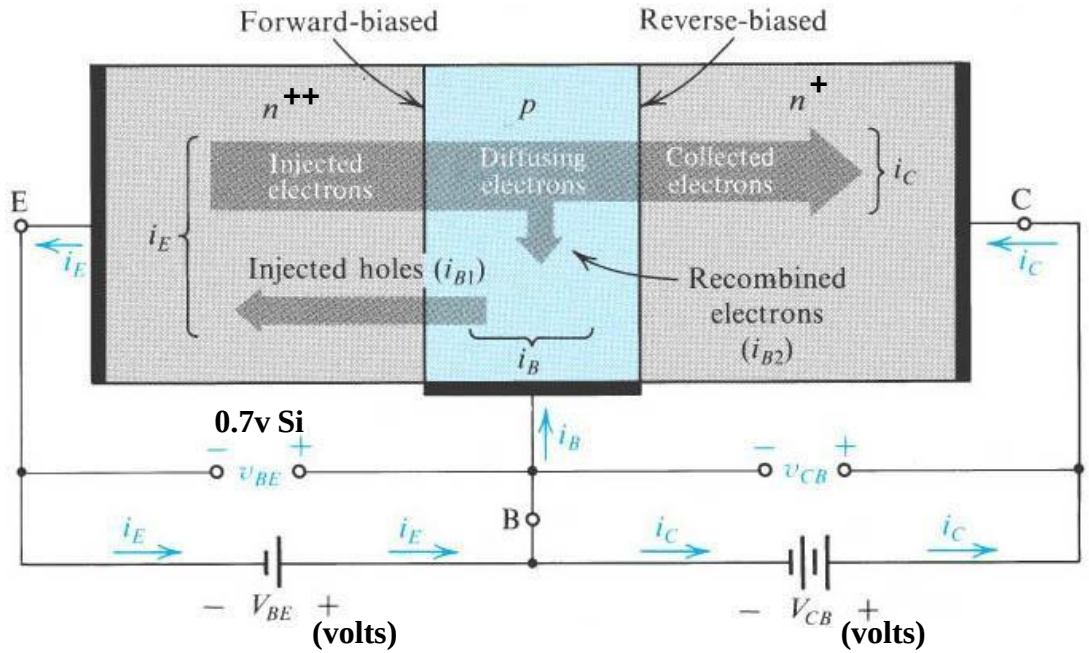
In this figure, the base-to-collector is in the situation of reversed biased.

Here, the flow of majority carriers is zero, Resulting in only a minority carrier flow.

Working or Operation of an NPN BJT







I_E is the Emitter Current due to the majority charge carriers (e-s in N-type Emitter) flowing from emitter towards collector through the base

I_E= 100% total current from emitter

I_B is the Base Current formed by the re-combination of the charge carriers entering the base from the emitter. Since the base is very lightly doped and is very thin , hence only a few re-combinations occur and the resultant base current is very small (µA) only about 2% of I_E.

I_C is the Collector Current formed by the fraction (98%) of majority charge carriers coming from the emitter plus some majority carriers present in the collector it self.

mA µA mA

$$I_E = I_B + I_C$$

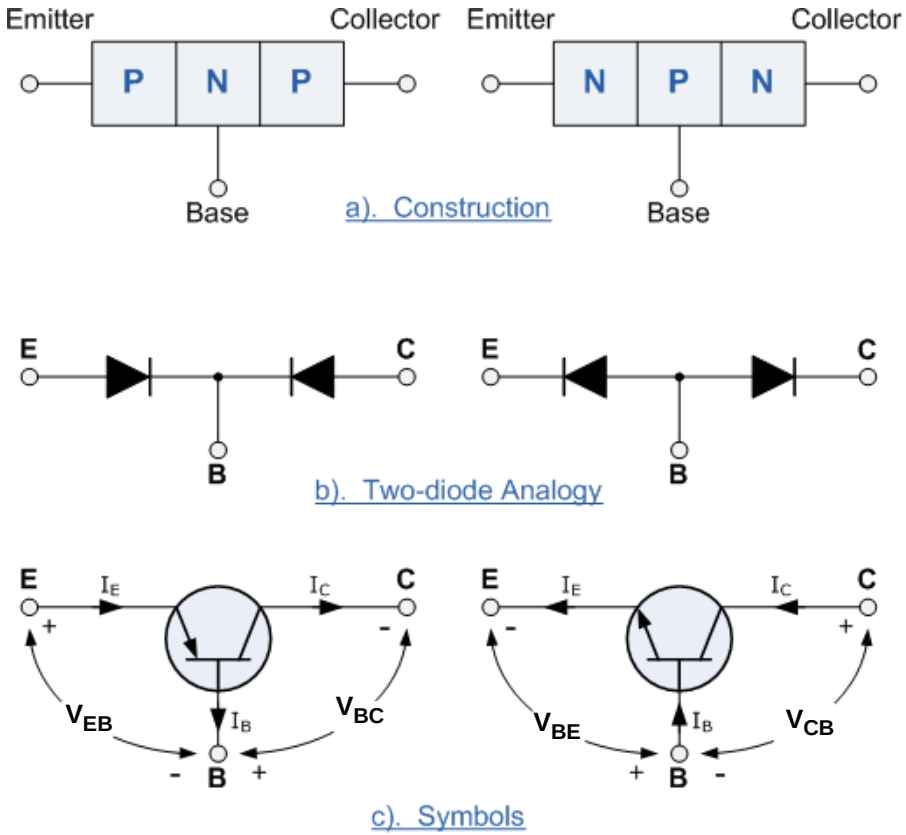
100% = 2% 98%

$$I_C = I_{C_{majority}} + I_{CO_{minority}}$$

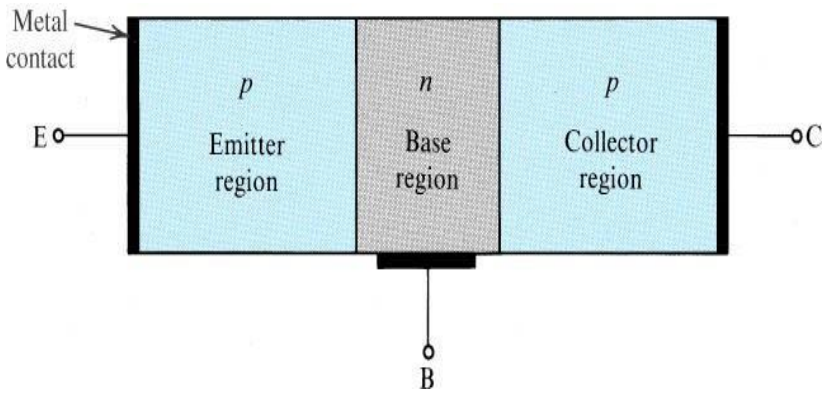
- $I_{CO} = I_C$ current with emitter terminal open and is

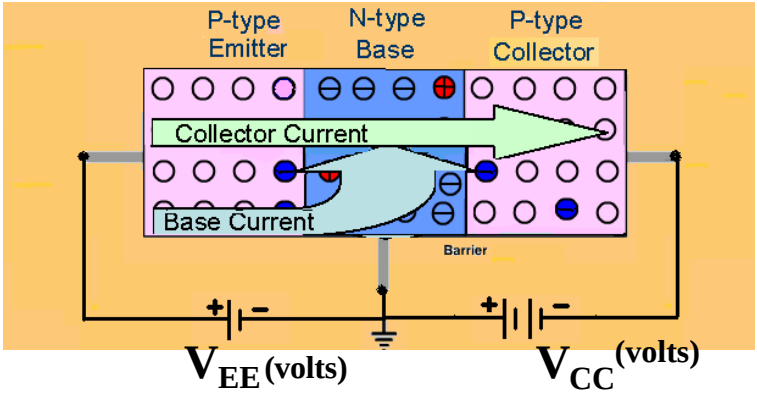
called leakage current.

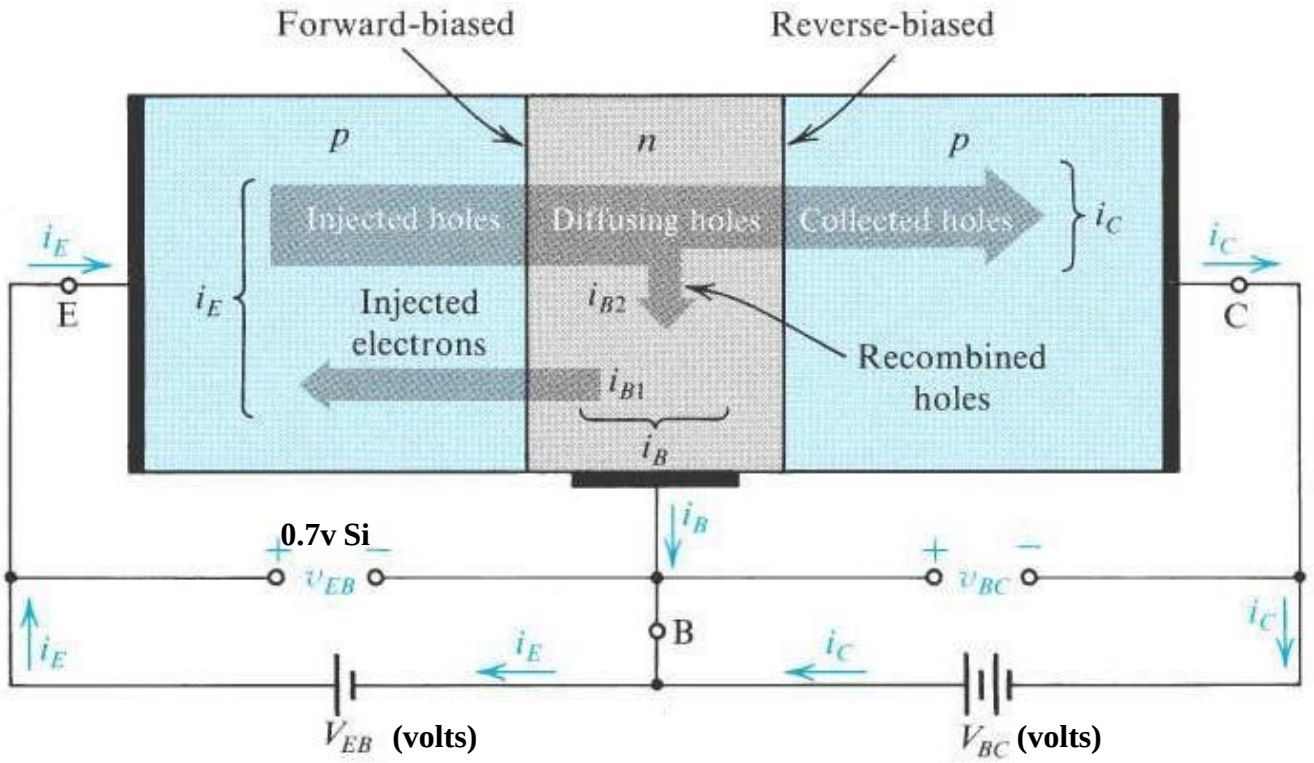
Polarity and Method of naming the voltage drops across the input and output junctions of PNP and NPN transistors:



Working or Operation of an PNP BJT



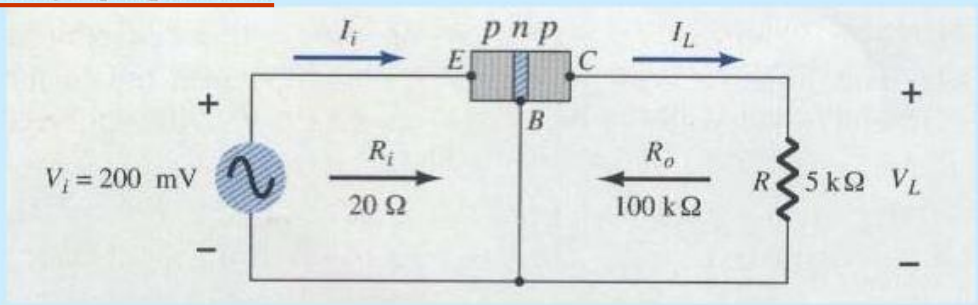




Ref: KFUPM

(volts)

Transistor Amplifying Action : Proof



$$I_i = \frac{V_i}{R_i} = \frac{200\text{ mV}}{20\ \Omega} = \mathbf{10\ mA}$$

Assume that $(I_c = I_e)$, Taking I_b = negligible

Also we know $I_e = I_b + I_c$

$$I_L = I_i = 10\text{ mA}$$

$$V_L = I_L R$$

$$= (10\text{ mA})(5\text{ k}\Omega)$$

$$= \mathbf{50\ V}$$

The voltage amplification is

$$A_v = \frac{V_L}{V_i} = \frac{50\text{ V}}{200\text{ mV}} = \mathbf{250}$$

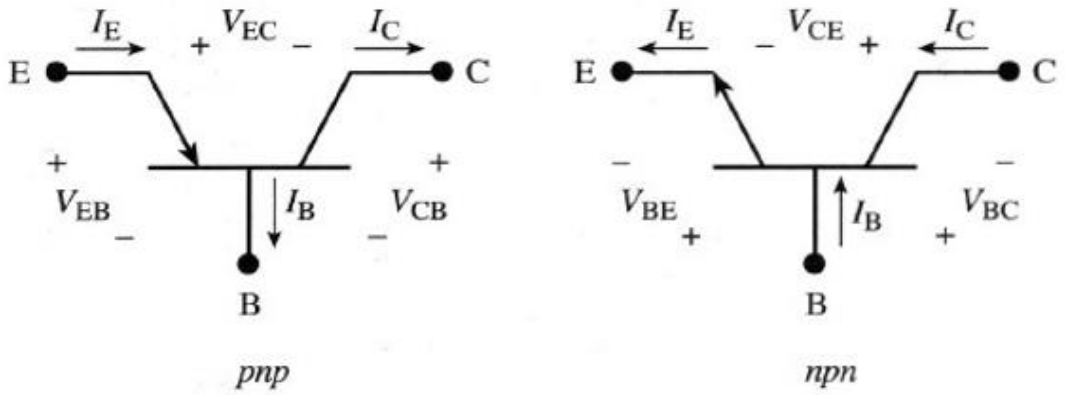
For the common-base configuration, the ac input resistance can be determined from the input characteristics curve, while

the ac output resistance can be determined from the output characteristics curve.

We will find that the input resistance is quite small typically varies from 10 to 100 Ohm (forward-biased), and

The output resistance is quite high typically varies from 50kiloOhm to 1 MegaOhm (reverse-biased).

Bipolar Junction Transistor Fundamentals



$$I_E = I_B + I_C$$

Transistor Configurations

There are 3 types of transistor connections or configuration in electric circuit:

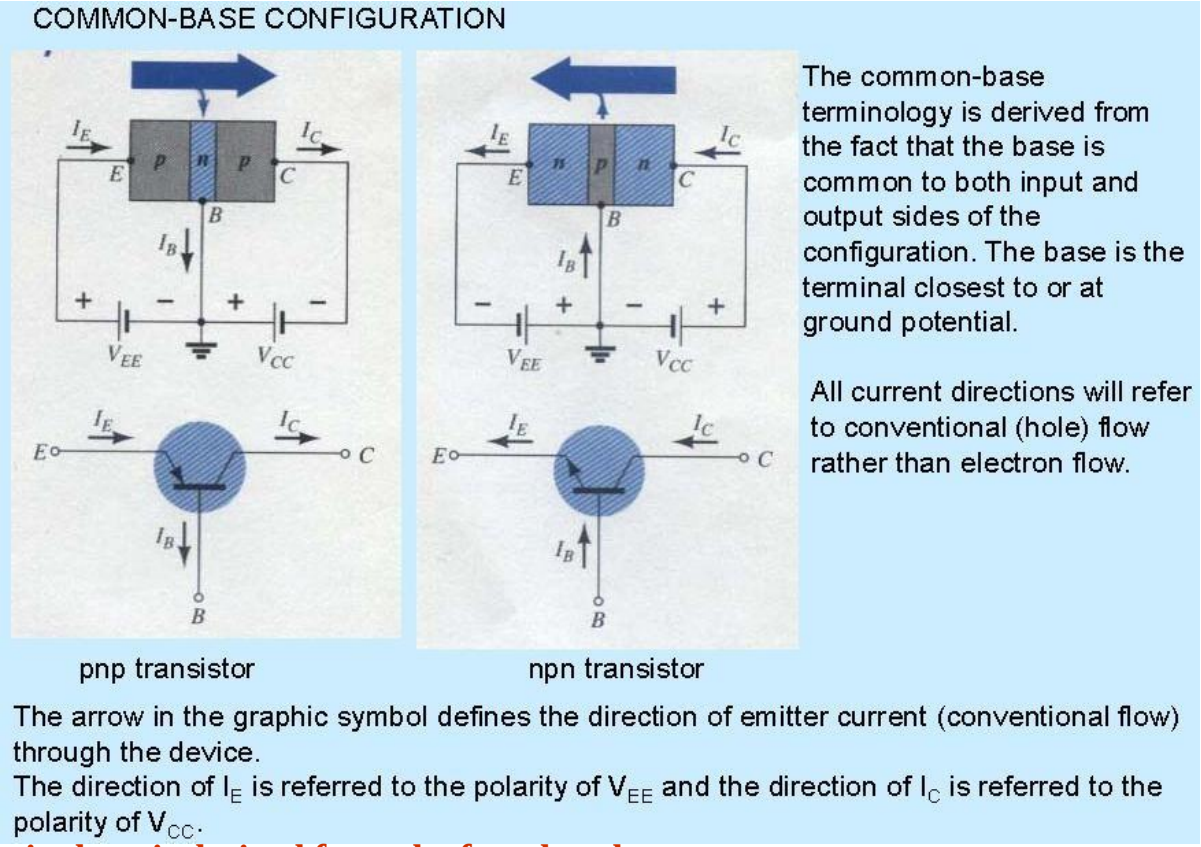
a) CB (common base)
b) CE (common emitter)
c) CC (common collector)

- **This configuration is based on which terminal is connected to the input signal and output signal.**
- **Table below shows the relationship between input signal and output signal with the transistor configuration.**

Configuration	Input terminal	Output terminal
CB	E	C
CE	B	C
CC	B	E

COMMON-BASE CONFIGURATION

Common-Base Configuration



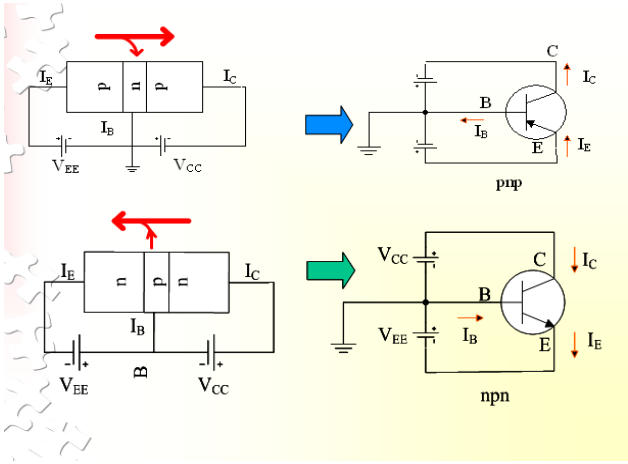
- **Common-base terminology is derived from the fact that the :**

  - base is common to both input and output of the configuration.

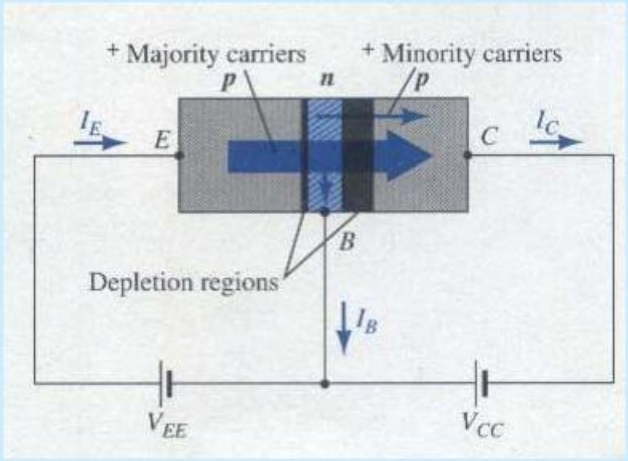
  - base is usually the terminal closest to or at ground potential.

- **All current directions will refer to conventional (hole) flow and the arrows in all electronic symbols have a direction defined by this convention.**

- **Note that the applied biasing (voltage sources) are such as to establish current in the direction indicated for each branch.**



CBC: Collector Current Expression and Current Amplification Factor ‘α’



Applying KCL law, we obtain

$$I_E = I_C + I_B$$

The collector current is comprised of two components- the majority and minority carriers. The minority current component is called the leakage current, Ico (Ic current with emitter terminal open).

The collector current is determined in total by

$$I_C = I_{C_{majority}} + I_{CO_{minority}}$$

Current Amplification Factor

Alpha (α)

Also $I_E = I_C + I_B$

$I_C \cong I_E$

But the base current I_B is only about 2% to 5% of the emitter current I_E hence very small in comparison to I_E and collector current I_C, hence

We know that the collector current is expressed as

$I_C = I_{C_{majority}} + I_{CO_{minority}}$

Is the fraction „α" of emitter current reaching the collector and the majority of carriers in collector

Leakage or minority carrier current and is vv small in comparison to the majority current hence can be neglected.

Thus, $\mathbf{I_C = \alpha I_E}$

$$\alpha = \frac{I_C}{I_E}$$

Is called the current amplification factor

In a dc mode, the levels of I_C and I_E due to the majority carriers are related by a quantity called alpha;

Is also called h_{FB} or large signal current gain for CB configuration

$$\alpha_{dc} = \frac{I_C}{I_E}$$

For $I_C \cong I_E$ alpha = 1

For practical devices the level of alpha typically extends from 0.90 to 0.998.

$$I_C = \alpha I_E + I_{CBO}$$

For ac mode where the points of operation moves on the characteristic curve, an ac alpha is defined by;

Change in collector current

$$\alpha_{ac} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}=\text{constant}}$$

Change in emitter current

Is also called h_{fb} or small signal ac current gain for CB configuration

For most situations, the magnitudes of dc alpha and ac alpha are quite close, Permitting the use of the magnitude of one for the other.

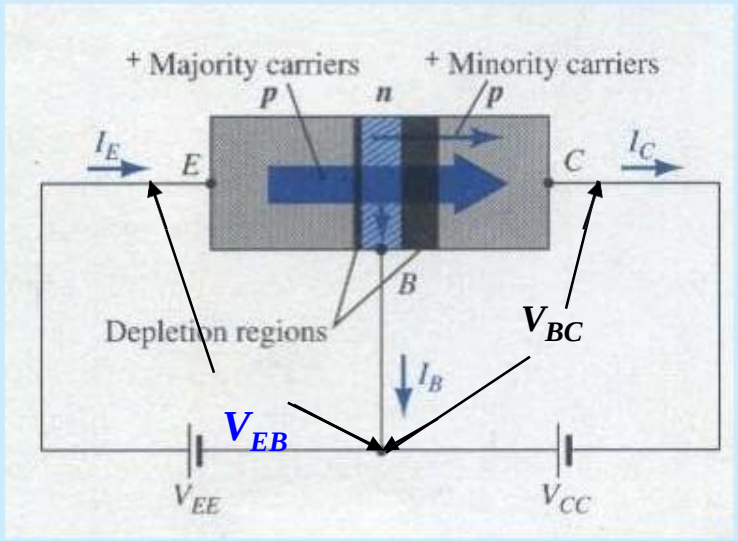
Common Base Voltage Gain

$$A_V = \frac{V_{OUT}}{V_{IN}}$$

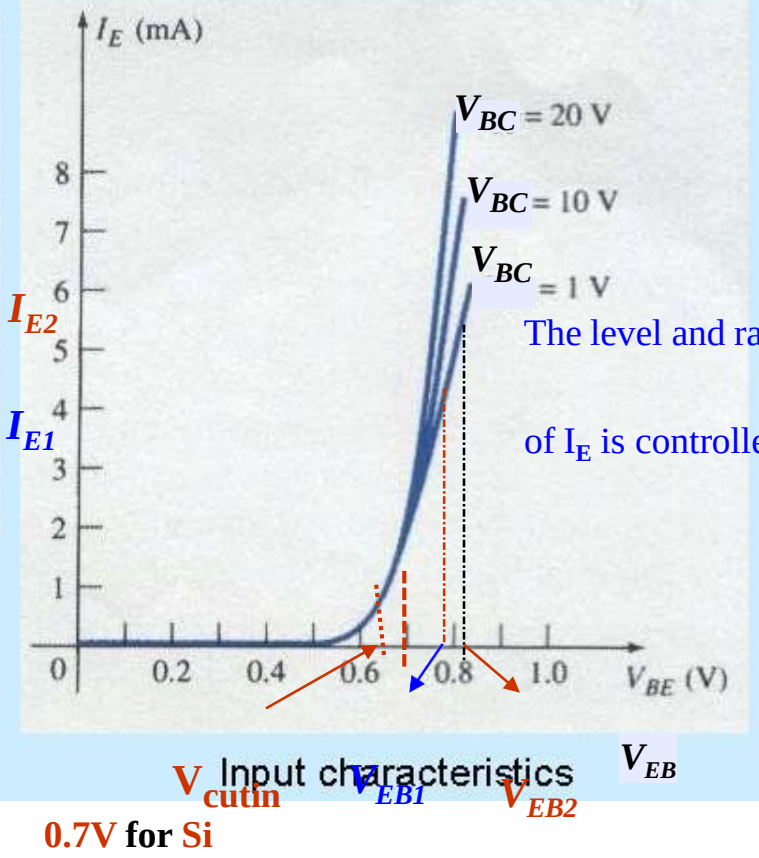
Characteristics of Common Base Configuration

Input Characteristics of CB Configuration

Input characteristics is the plot of I_E - vs - V_{EB} with output voltage V_{BC} remaining constant



Biasing pnp transistor (CB)



The level and rate of change of I_E is controlled by V_{BC}

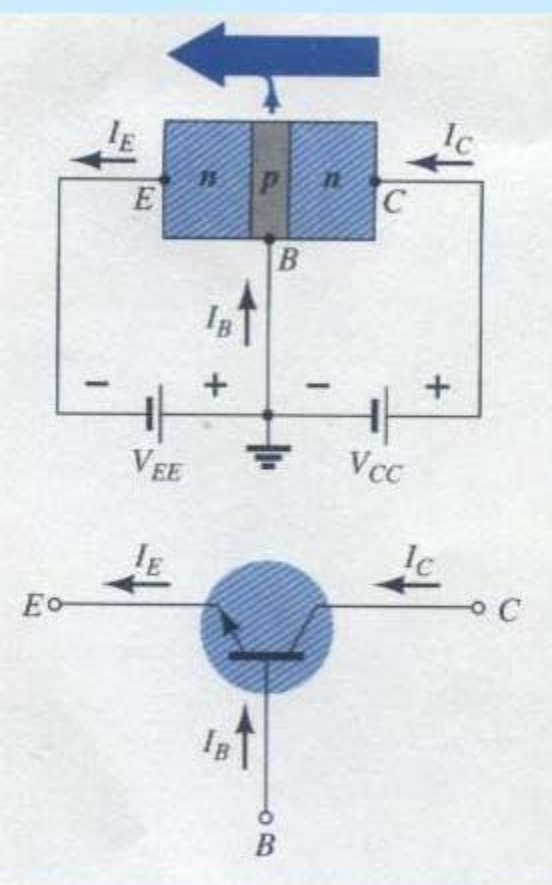
0.7V for Si

Conduction starts when V_{EB}=0.7V considering Si transistor as the input junction becomes FB at this voltage.

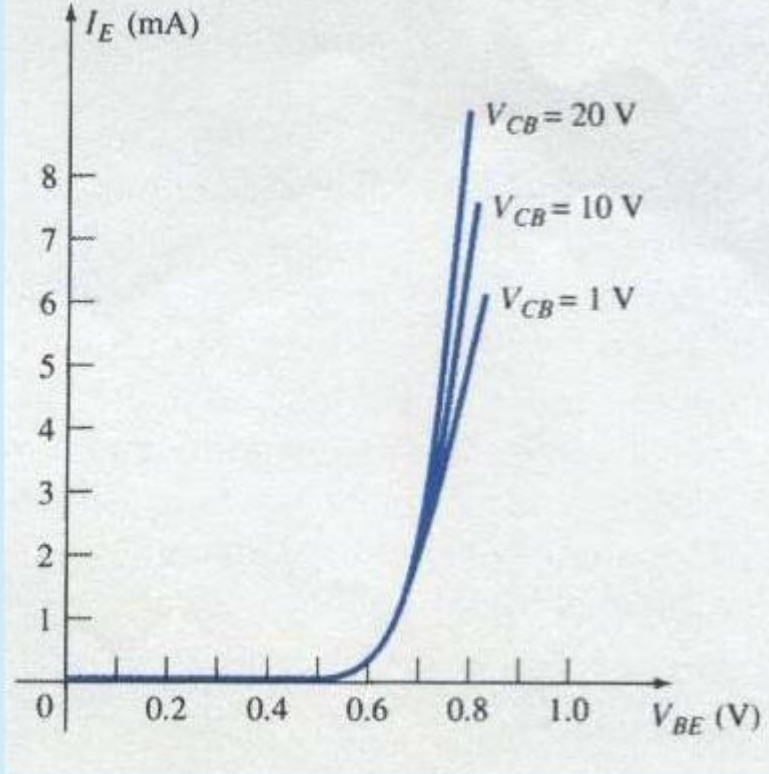
Hence the input characteristics is same as that of a Forward Biased PN-junction.

The transistor input resistance can be expressed as:

NPN CB Configuration:



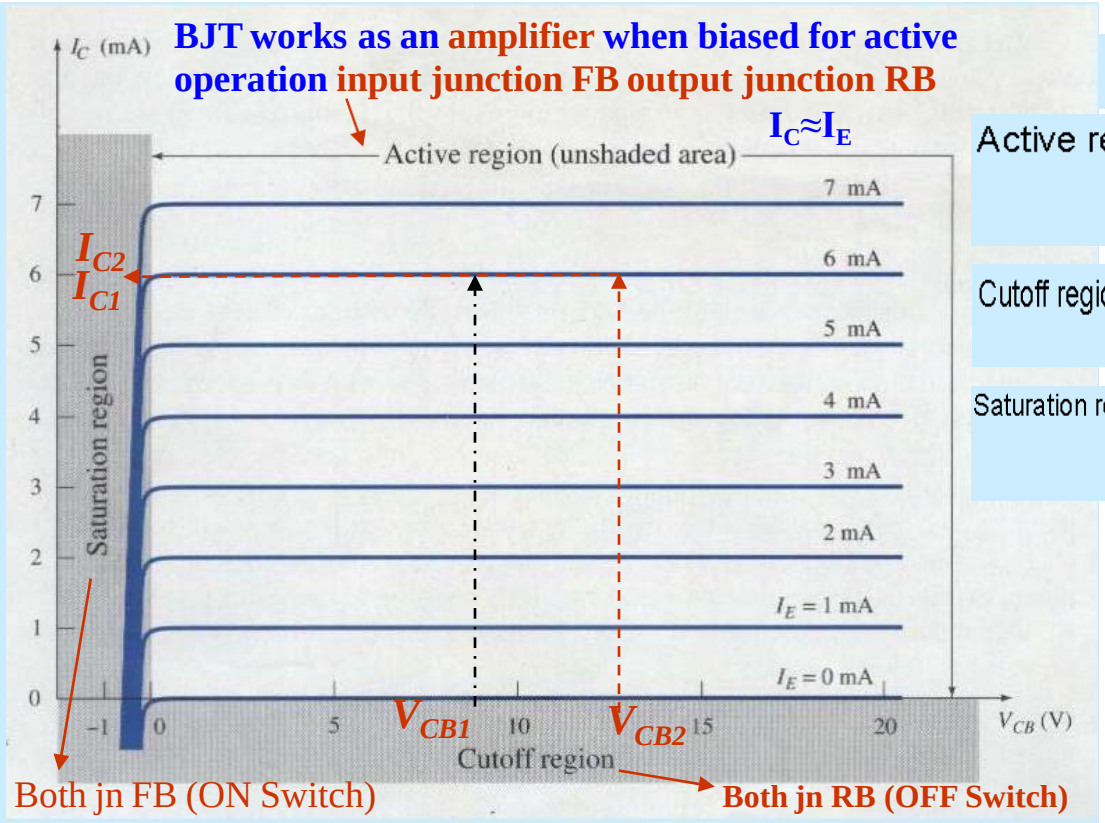
Biasing npn transistor (CB)



Input characteristics

Common Base Configuration: Output Characteristics

Output characteristics is the plot of I_C vs V_{CB} with input current I_E remaining constant



Output characteristics

$I_C = I_{Cmaxm}$ $\quad$ $I_C = I_{CBO}$

$I_E = I_C + I_B$

The level of I_C will be controlled by I_E

3 Regions

Active region : the base-emitter junction is forward-biased, while the collector-base junction is reverse -biased. $I_C \approx I_E$

Cutoff region : the base-emitter junction and the collector-base junction are both reverse-biased. $I_C = I_{CBO}$

Saturation region : the region of the characteristics in the left of V_{CB} = 0V. The base-emitter junction and the collector-base junction are both forward-biased. $I_C = I_{Cmaxm}$

Output resistance r_o

The output resistance r_o is high because input junction is RB.

Also, from the curve it can be seen that the characteristic is absolutely flat indicating constant I_C.

This means that is there is no change in output current with variation in output voltage which indicates a very high resistance at the output.

r_o is very high, varies from about 1MΩ to about 10MΩ.

α and β Relationship in a NPN Transistor

$$\text{DC Current Gain} = \frac{\text{Output Current}}{\text{Input Current}} = \frac{I_C}{I_B}$$

$$I_E = I_B + I_C \ldots\ldots \text{(KCL)} \quad \text{and} \quad \frac{I_C}{I_E} = \alpha$$

$$\text{Thus:} \quad I_B = I_E - I_C$$

$$I_B = I_E - \alpha I_E$$

$$I_B = I_E (1 - \alpha)$$

$$\therefore \quad \beta = \frac{I_C}{I_B} = \frac{I_C}{I_E(1-\alpha)} = \frac{\alpha}{1-\alpha}$$

By combining the two parameters α and β we can produce two mathematical expressions that gives the relationship between the different currents flowing in the transistor.

$$\alpha = \frac{\beta}{\beta + 1} \quad \text{or} \quad \alpha = \beta(1-\alpha)$$

$$\beta = \frac{\alpha}{1-\alpha} \quad \text{or} \quad \beta = \alpha(1+\beta)$$

$$\text{If} \quad \alpha = 0.99 \qquad \beta = \frac{0.99}{0.01} = 99$$

The values of Beta vary from about 20 for high current power transistors to well over 1000 for high frequency low power type bipolar transistors. The value of Beta for most standard NPN transistors can be found in the manufactures data sheets but generally range between 50 – 200.

CB Output Characteristics: Regions of Operation

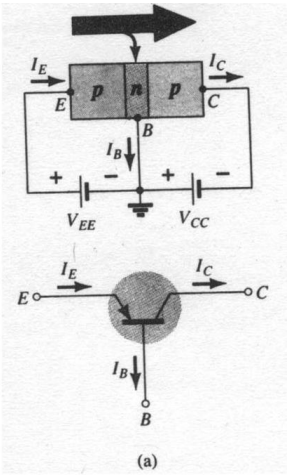
Active region	Saturation region	Cut-off region
• I_E increased, Ic increased • BE junction forward bias and CB junction reverse bias • Refer to the graf, Ic ≈ I_E • Ic not depends on V_{CB} • Suitable region for the transistor working as **voltage** amplifier	• BE and CB junction is forward bias • Small changes in V_{CB} will cause big different to Ic • The allocation for this region is to the left of V_{CB}= 0 V.	• Region below the line of I_E=0 A • BE and CB is reverse bias • no current flow at collector, only leakage current

$$I_E = I_B + I_C$$

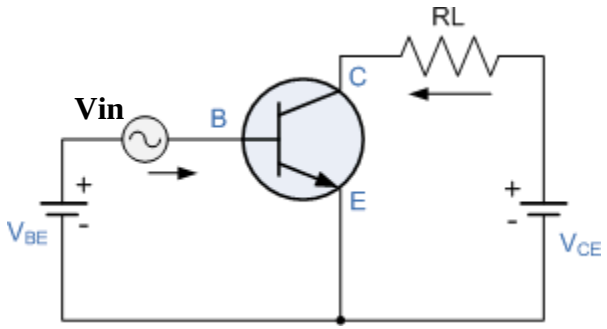
Current in base is negligible.
Current in emitter and collector is almost same.

Current gain less than unity

$$\alpha = I_C/I_E \ (0.90 - 0.998)$$



COMMON-EMITTER CONFIGURATION



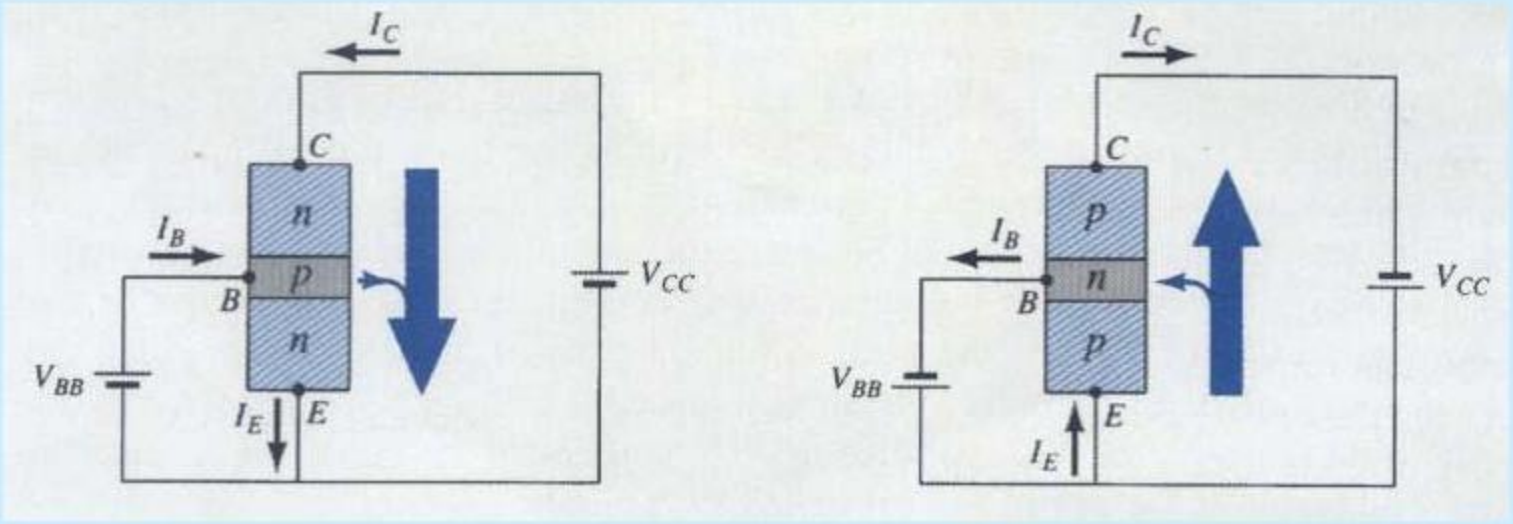
Common-emitter configuration (CE)

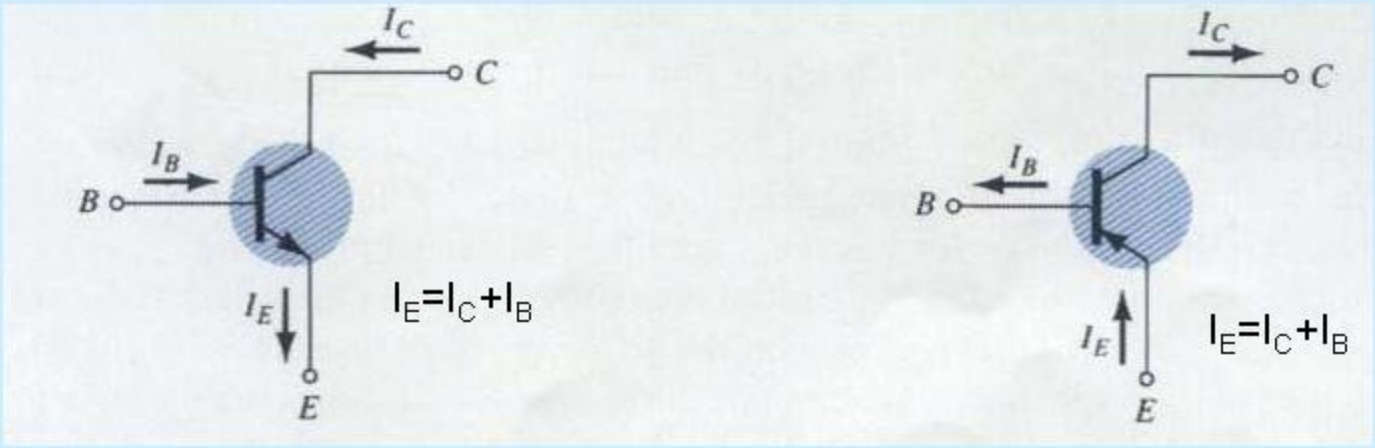
- **It is called common-emitter configuration since :**
  - **emitter is common or reference to both i/p and o/p terminals.**
  - **emitter is usually the terminal closest to or at ground potential.**

- **Almost all amplifier design is using CE configuration due to the high gain for current and voltage.**

- **Two set of characteristics are necessary to describe the behavior for CE ;input (base terminal) and output (collector terminal) parameters.**

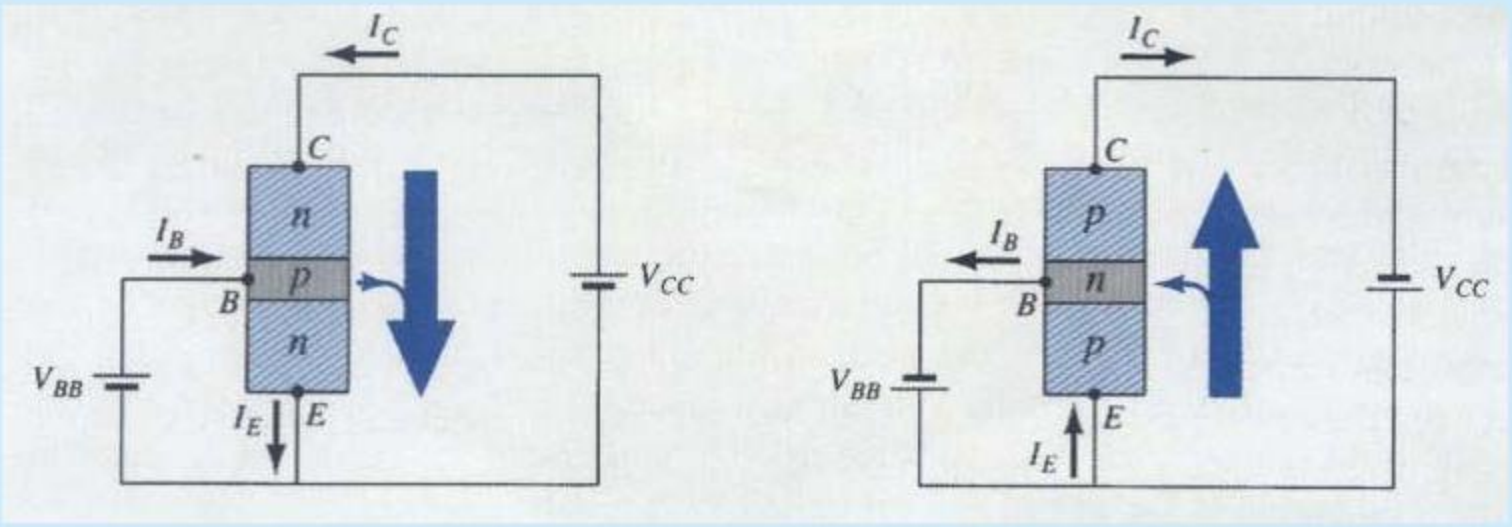
Common Emitter Configuration: Biasing arrangements

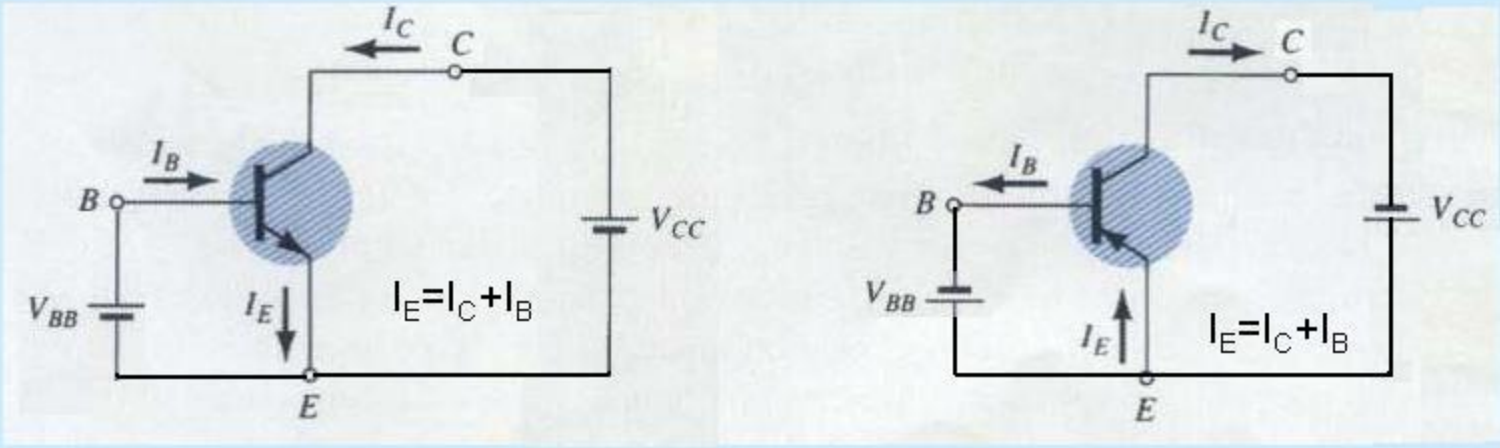




In this configuration, the emitter is common or reference to both the input and output Terminals. In this case, common to both the base and collector terminals.

Biasing in active mode with symbolic representations:



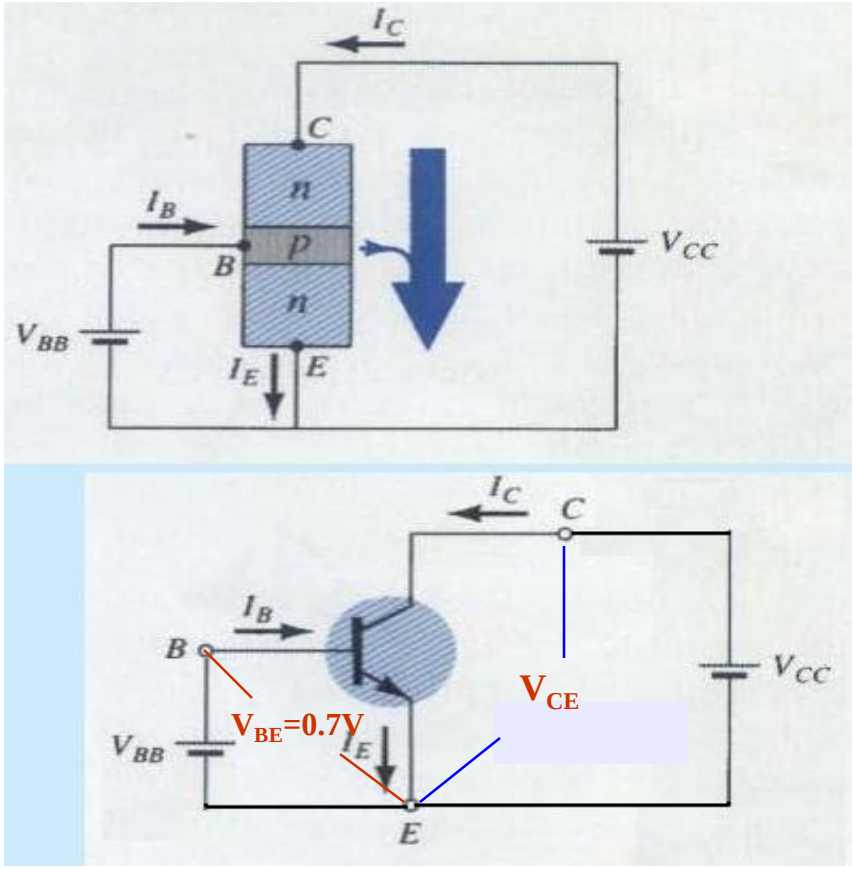


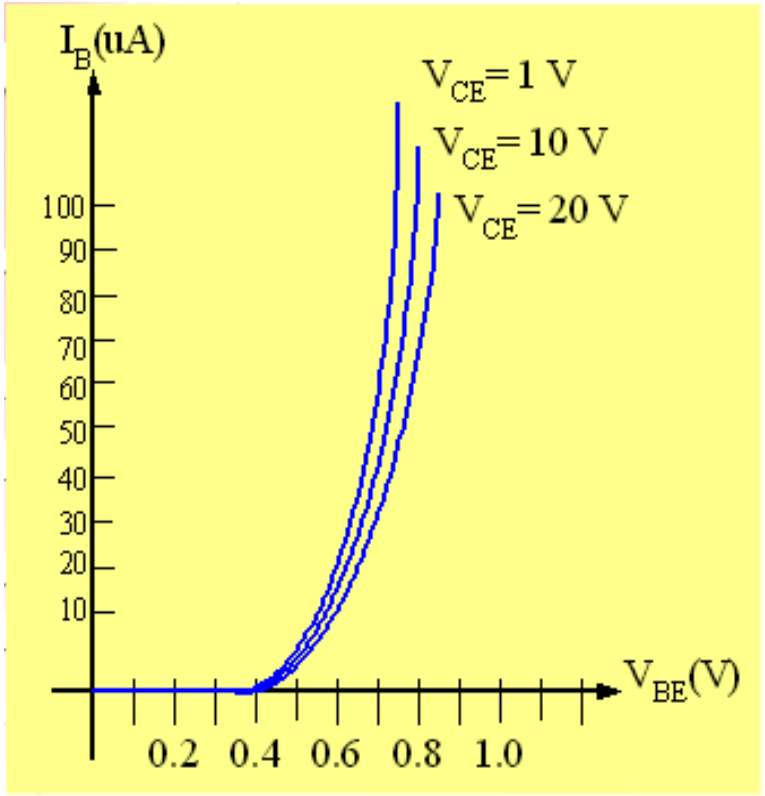
In this configuration, the emitter is common or reference to both the input and output Terminals. In this case, common to both the base and collector terminals.

Input /Output characteristics of CE Amplifier

- **To describe the behavior of common-emitter amplifiers two sets of characteristics are required :**
  - **Input or driving point characteristics.**
  - **Output or collector characteristics**
- **The output characteristics has 3 basic regions depending on the biasing arrangements:**
  - **Active region –defined by the biasing arrangements (input jn FB –Output jn RB)**
  - **Cutoff region – region where the collector current is 0A (input jn RB –Output jn RB)**
  - **Saturation region- region of the characteristics to the left of $V_{CB} = 0V$ (input jn FB – Output jn FB)**

Input Characteristics of CE Configuration

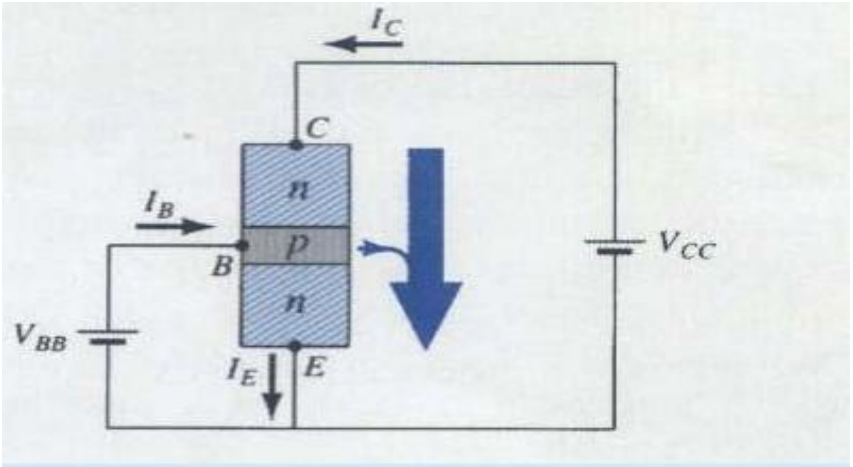


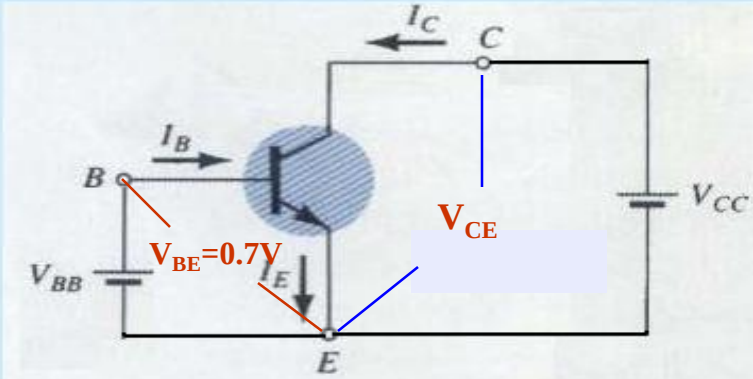


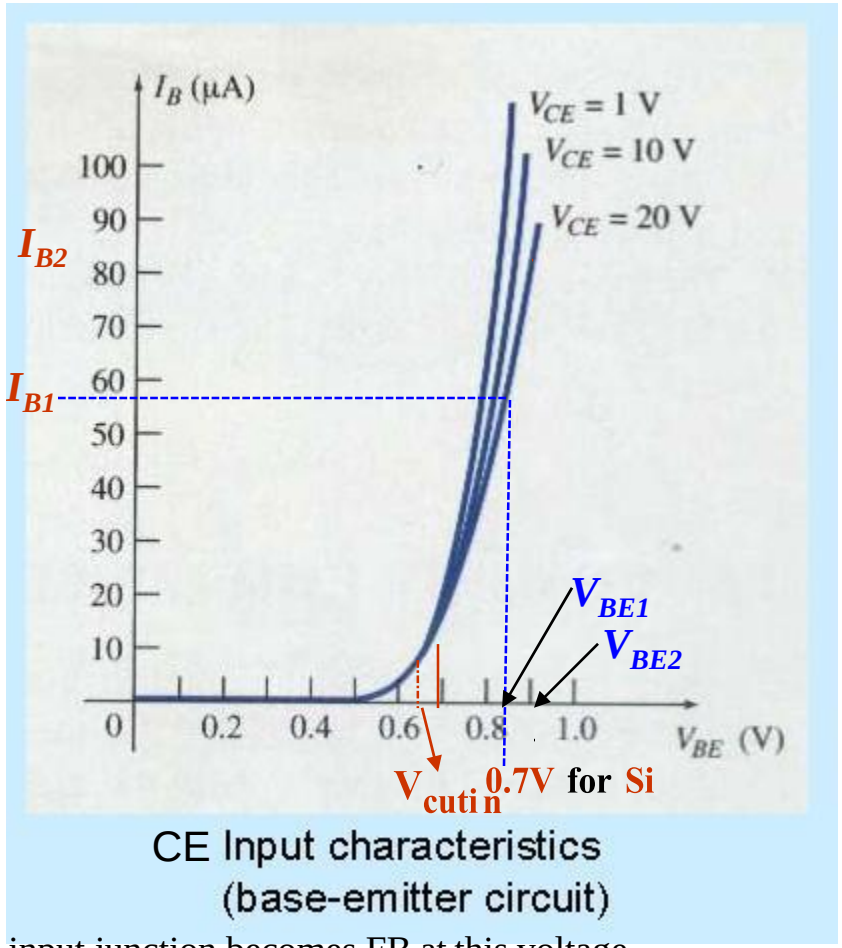
Input characteristics for a common-emitter NPN transistor

- **I_B is microamperes compared to milliamperes of I_C.**
- **I_B will flow when V_{BE} > 0.7V that is when the input jn or the base-emitter junction is forward biased for silicon and 0.3V for germanium**
- **Before this value I_B is very small and no I_B flows.**
- **Base-emitter junction is forward bias at V_{BE} > 0.7V and current conduction starts.**
- **The input characteristics is that of a FB PN-jn diode.**
- **Increasing V_{CE} will reduce I_B for different values.**

Input Characteristics of CE Configuration



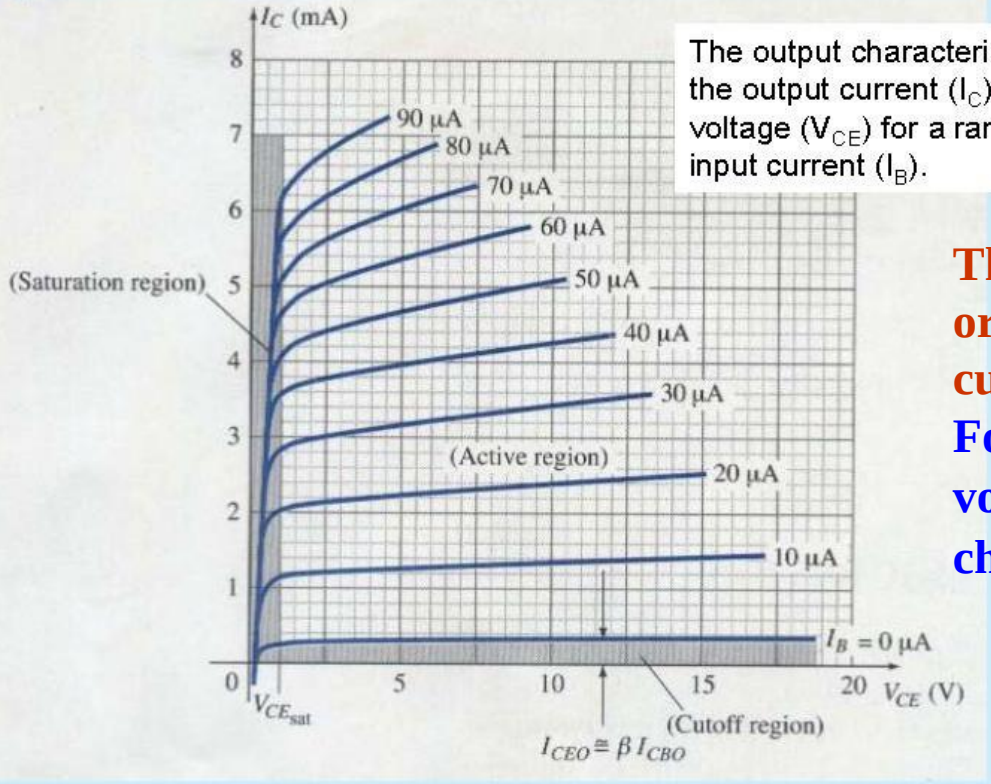




Conduction starts when V_{BE}=0.7V considering Si transistor as the input junction becomes FB at this voltage.

Hence the input characteristics is same as that of a Forward Biased PN-junction.

CE Configuration: Output Characteristics



The output characteristics are a plot of the output current (I_C) versus the output voltage (V_{CE}) for a range of values of input current (I_B).

Output characteristics (collector-emitter circuit)

The output characteristics is almost flat or constant for a particular value of input current I_B.

For a large variation in Collector emitter voltage V_{CE} there is only a very small change in collector current I_C.

This indicates that the collector current I_C is slightly controllable by variation in collector-emitter voltage V_{CE}

3 Regions

Active region : the base-emitter junction is forward-biased, while the collector-base junction is reverse -biased. $I_C \approx I_E$

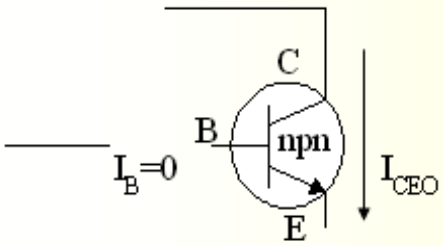
Cutoff region : the base-emitter junction and the collector-base junction are both reverse-biased. $I_C = I_{CEO}$ Or $I_C = \beta I_{CBO}$

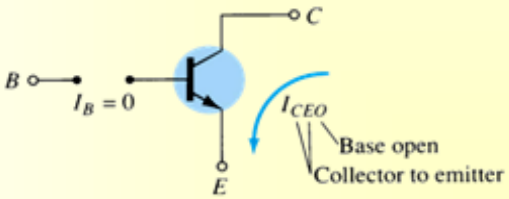
Saturation region : the region of the characteristics in the left of $V_{CB} = 0V$. The base-emitter junction and the collector-base junction are both forward-biased. $I_C = I_{Cmaxm}$

CE Output Characteristics: Regions of Operation

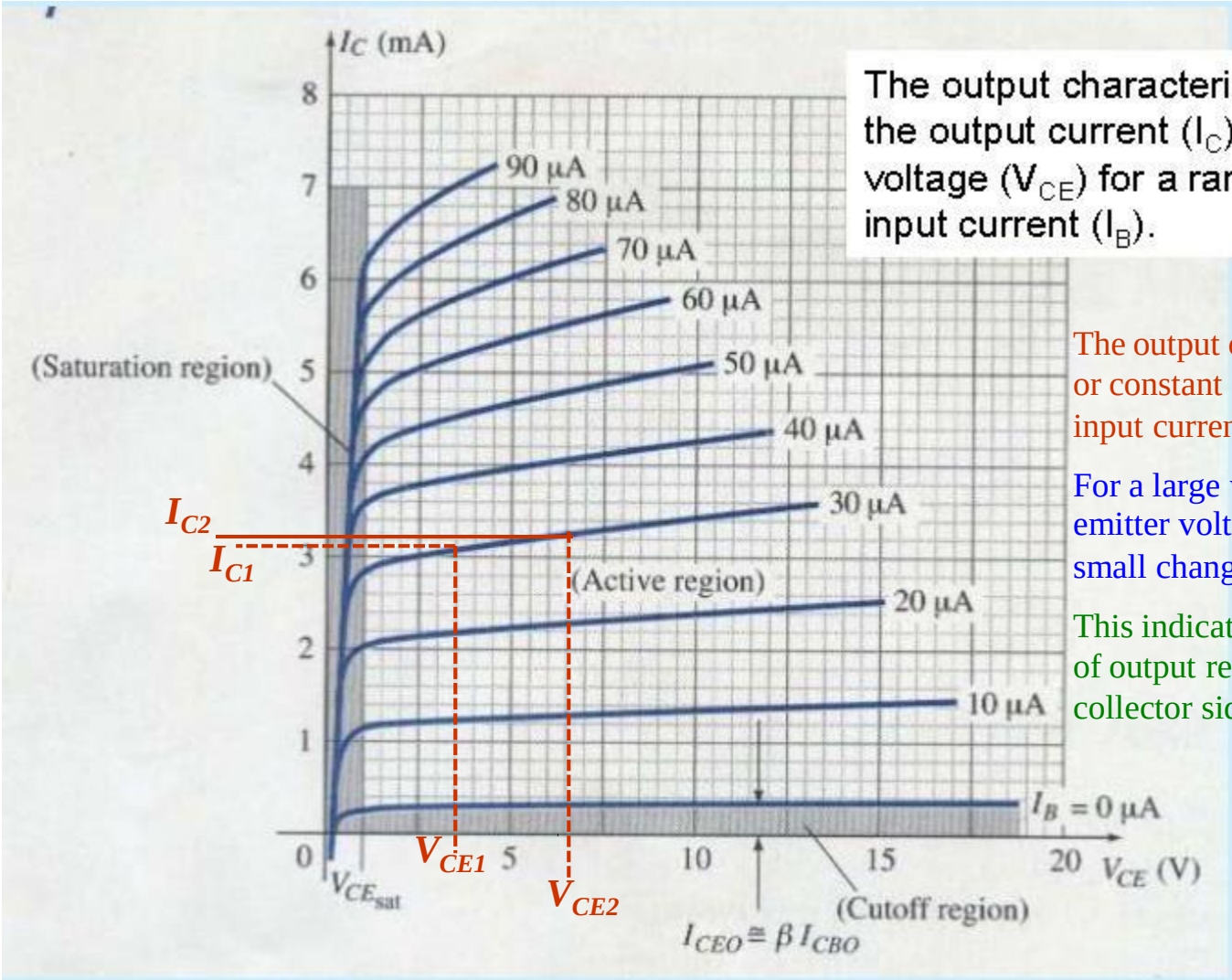
- **For small V_{CE} ($V_{CE} < V_{CESAT}$, I_C increase linearly with increasing of V_{CE}**
- **$V_{CE} > V_{CESAT}$ I_C not totally depends on V_{CE} → constant I_C**
- **I_B(μA) is very small compare to I_C (mA). Small increase in I_B cause big increase in I_C**
- **I_B=0 A → I_{CEO} flows.**
- **Noticing the value when I_C=0A. There is still some value of current flows.**

Active region	Saturation region	Cut-off region
• B-E junction is forward bias • C-B junction is reverse bias • can be employed for voltage, current and power amplification	• B-E and C-B junction is forward bias, thus the values of I_B and I_C is too big. • The value of V_{CE} is so small. • Suitable region when the transistor as a logic switch. • NOT and avoid this region when the transistor as an amplifier.	• region below I_B=0μA is to be avoided if an undistorted o/p signal is required • B-E junction and C-B junction is reverse bias • I_B=0, I_C not zero, during this condition I_C=I_{CEO} where is this current flow when B-E is reverse bias.





CE Configuration: Output Characteristics & Output Resistances



The output characteristics are a plot of the output current (I_C) versus the output voltage (V_{CE}) for a range of values of input current (I_B).

The output characteristics is almost flat or constant for a particular value of input current I_B.

For a large variation in Collector emitter voltage V_{CE} there is only a very small change in collector current I_C.

This indicates that there is a small value of output resistance offered by the collector side. **about to 10KΩ**

Output characteristics (collector-emitter circuit)

Beta

In a dc mode, the levels of I_C and I_B are related by aquantity called beta;

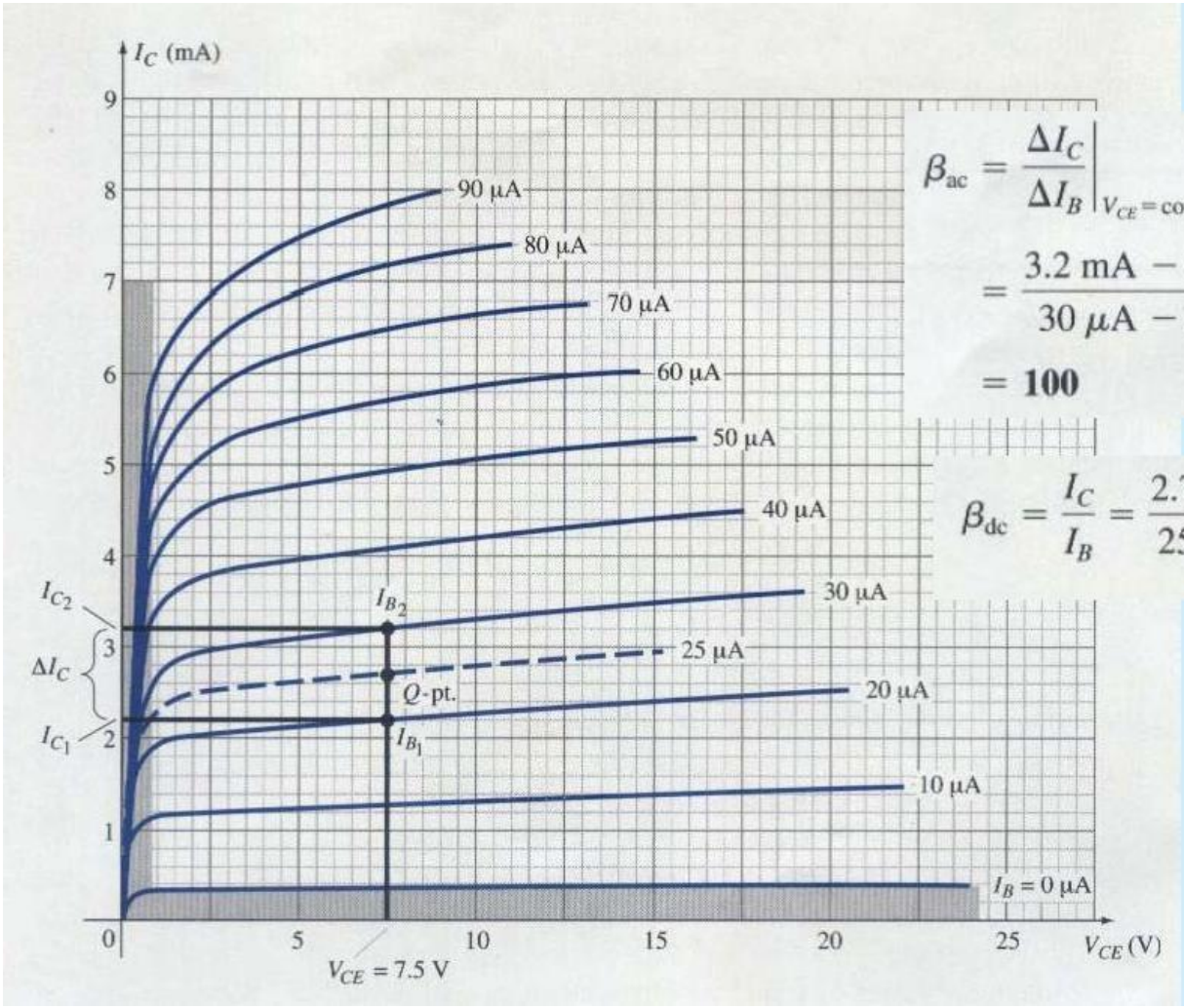
$$\beta_{dc} = \frac{I_C}{I_B}$$

For $I_C \cong I_E$ alpha = 1

For practical devices the level of beta typically extends from 50 to 400.

For ac mode where the points of operation moves on the characteristic curve, an ac beta is defined by;

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}}$$



$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}} = \frac{I_{C_2} - I_{C_1}}{I_{B_2} - I_{B_1}}$$

$$= \frac{3.2\text{ mA} - 2.2\text{ mA}}{30\ \mu\text{A} - 20\ \mu\text{A}} = \frac{1\text{ mA}}{10\ \mu\text{A}}$$

$$= \mathbf{100}$$

$$\beta_{dc} = \frac{I_C}{I_B} = \frac{2.7\text{ mA}}{25\ \mu\text{A}} = \mathbf{108}$$

Note that;
Value of beta ac
is close
to beta dc.

Beta (β) or amplification factor

- **The ratio of dc collector current (IC) to the dc base current (IB) is dc beta (βdc) which is dc current gain where IC and IB are determined at a particular operating point, Q-point (quiescent point).**
- **It's define by the following equation:**

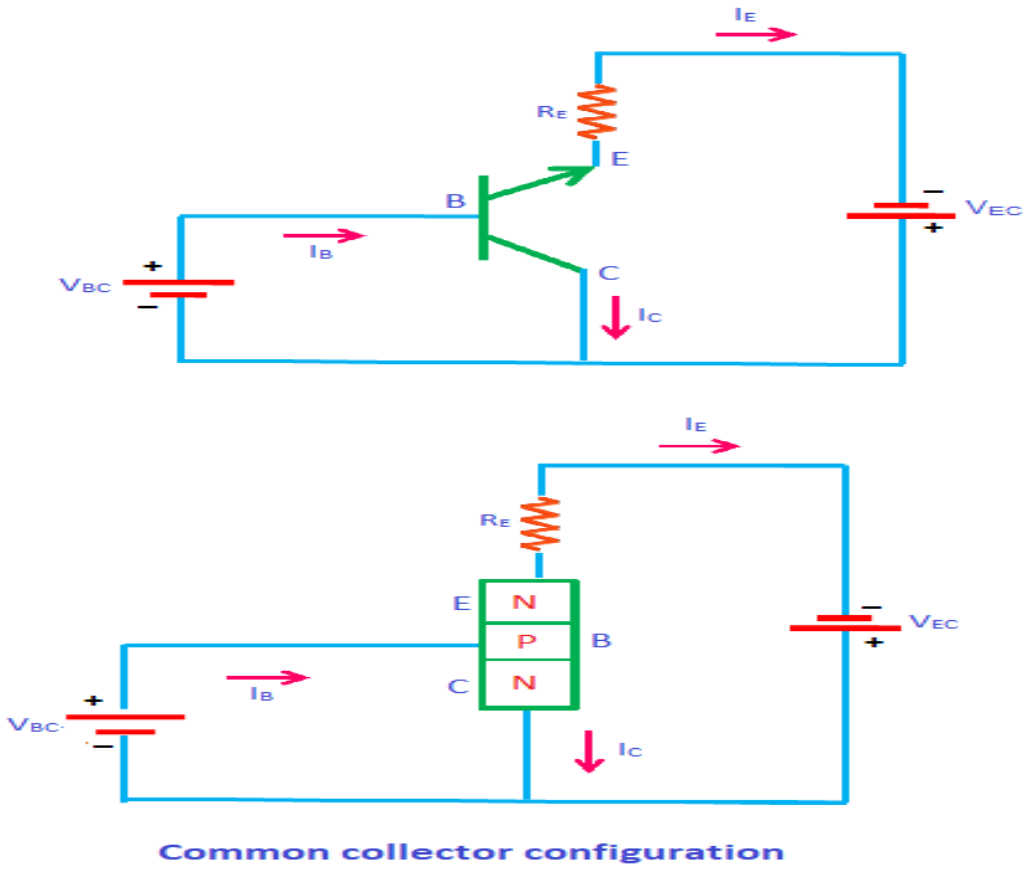
  $30 < \beta dc < 300 \rightarrow$ 2N3904

- **On data sheet, $\beta_{dc}=h_{FE}$ with *h* is derived from ac hybrid equivalent circuit. h_{FE} are derived from forward-current amplification and common-emitter configuration respectively.**

- **For ac conditions an ac beta has been defined as the changes of collector current (I_C) compared to the changes of base current (I_B) where I_C and I_B are determined at operating point.**
- **On data sheet, $\beta_{ac}=h_{fe}$**
- **It can defined by the following equation**

Common Collector Configuration

In this configuration, the base terminal of the transistor serves as the input, the emitter terminal is the output and the collector terminal is common for both input and output. Hence, it is named as common collector configuration. The input is applied between the base and collector while the output is taken from the emitter and collector. In common collector configuration, the collector terminal is grounded so the common collector configuration is also known as grounded collector configuration.



Common collector configuration

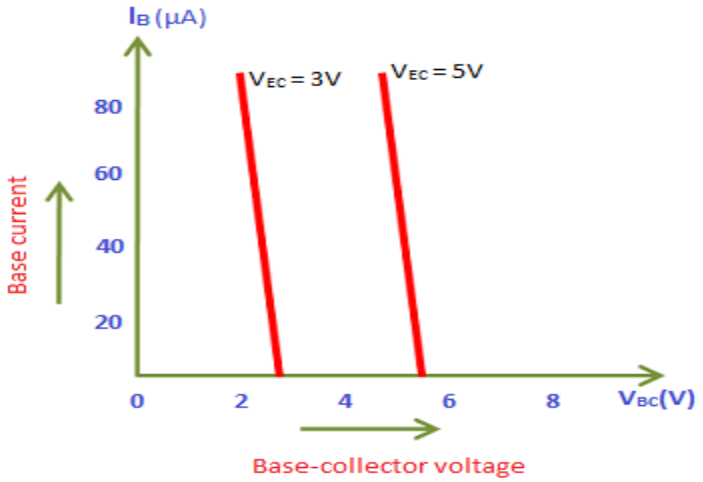
Sometimes common collector configuration is also referred to as emitter follower, voltage follower, common collector amplifier, CC amplifier, or CC configuration. This configuration is mostly used as a voltage buffer.The input supply voltage between base and collector is denoted by V_{BC} while the output voltage between emitter and collector is denoted by V_{EC}.

In this configuration, input current or base current is denoted by I_B and output current or emitter current is denoted by I_E. The common collector amplifier has high input impedance and low output impedance. It has low voltage gain and high current gain. The power gain of the common collector amplifier is medium. To fully describe the behavior of a transistor with CC configuration, we need two set of characteristics - input characteristics and output characteristics.

Input characteristics

The input characteristics describe the relationship between input current or base current (I_B) and input voltage or base-collector voltage (V_{BC}).
First, draw a vertical line and a horizontal line. The vertical line represents y-axis and horizontal line represents x-axis
The input current or base current (I_B) is taken along y-axis (vertical line) and the input voltage or base-collector voltage (V_{BC}) is taken along x-axis (horizontal line).

To determine the input characteristics, the output voltage V_{EC} is kept constant at 3V and the input voltage V_{BC} is increased from zero volts to different voltage levels. For each level of input voltage $V_{BC,}$ the corresponding input current I_B is noted. A curve is then drawn between input current I_B and input voltage V_{BC} at constant output voltage V_{EC} (3V).



Input characteristics

Next, the output voltage V_{EC} is increased from 3V to different voltage level, say for example 5V and then kept constant at 5V. While increasing the output voltage V_{EC}, the input voltage V_{BC} is kept constant at zero volts.

After we kept the output voltage V_{EC} constant at 5V, the input voltage V_{BC} is increased from zero volts to different voltage levels. For each level of input voltage V_{BC}, the corresponding input current I_B is noted. A curve is then drawn between input current I_B and input voltage V_{BC} at constant output voltage V_{EC} (5V). This process is repeated for higher fixed values of output voltage (V_{EC}).

Output characteristics

The output characteristics describe the relationship between output current or emitter current (I_E) and output voltage or emitter-collector voltage (V_{EC}). First, draw a vertical line and a horizontal line. The vertical line represents y-axis and horizontal line represents x-axis.

The output current or emitter current (I_E) is taken along y-axis (vertical line) and the output voltage or emitter-collector voltage (V_{EC}) is taken along x-axis (horizontal line).

To determine the output characteristics, the input current I_B is kept constant at zero micro amperes and the output voltage V_{EC} is increased from zero volts to different voltage levels. For each level of output voltage V_{EC}, the corresponding output current I_E is noted. A curve is then drawn between output current I_E and output voltage V_{EC} at constant input current I_B (0 μA).

Output characteristics

Next, the input current (I_B) is increased from 0 µA to 20 µA and then kept constant at 20 µA. While increasing the input current (I_B), the output voltage (V_{EC}) is kept constant at 0 volts.

After we kept the input current (I_B) constant at 20 µA, the output voltage (V_{EC}) is increased from zero volts to different voltage levels. For each level of output voltage (V_{EC}), the corresponding output current (I_E) is recorded. A curve is then drawn between output current I_E and output voltage V_{EC} at constant input current I_B (20µA). This region is known as the active region of a transistor. This process is repeated for higher fixed values of input current I_B (I.e. 40 µA, 60 µA, 80 µA and so on).

In common collector configuration, if the input current or base current is zero then the output current or emitter current is also zero. As a result, no current flows through the transistor. So the transistor will be in the cutoff region. If the base current is slightly increased then the output current or emitter current also increases. So the transistor falls into the active region. If the base current is heavily increased then the current flowing through the transistor also heavily increases. As a result, the transistor falls into the saturation region.

TRANSISTOR BIASING, DC LOAD LINE,QUIESCENT POINT

The proper flow of zero signal collector current and the maintenance of proper collector-emitter voltage during the passage of signal is known as **Transistor Biasing**. The circuit which provides transistor biasing is called as **Biasing Circuit**.

Need for DC biasing

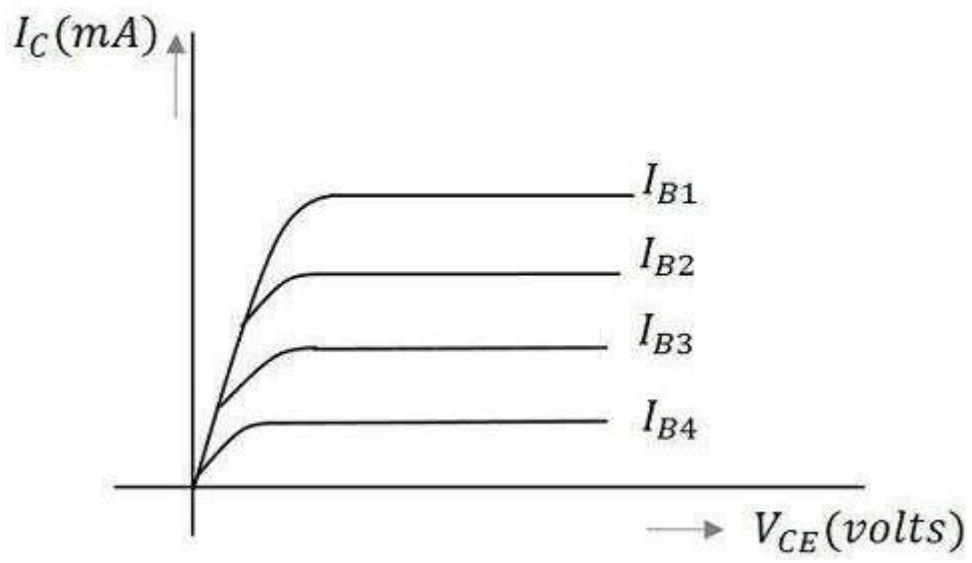
If a signal of very small voltage is given to the input of BJT, it cannot be amplified. Because, for a BJT, to amplify a signal, two conditions have to be met.

- The input voltage should exceed **cut-in voltage** for the transistor to be **ON**.
- The BJT should be in the **active region**, to be operated as an **amplifier**.

If appropriate DC voltages and currents are given through BJT by external sources, so that BJT operates in active region and superimpose the AC signals to be amplified, then this problem can be avoided. The given DC voltage and currents are so chosen that the transistor remains in active region for entire input AC cycle. Hence DC biasing is needed.

Output Characteristics

When the output characteristics of a transistor are considered, the curve looks as below for different input values.



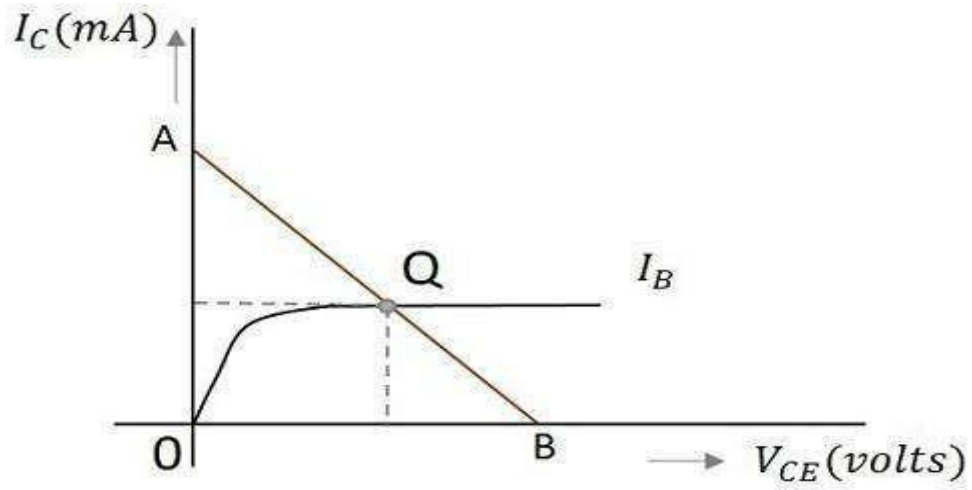
In the above figure, the output characteristics are drawn between collector current **IC** and collector voltage **VCE** for different values of base current **IB**. These are considered here for different input values to obtain different output curves.

Operating point

When a value for the maximum possible collector current is considered, that point will be present on the Y-axis, which is nothing but the **saturation point**. As well, when a value for the maximum possible collector emitter voltage is considered, that point will be present on the X-axis, which is the **cutoff point**.

When a line is drawn joining these two points, such a line can be called as **Load line**. This is called so as it symbolizes the output at the load. This line, when drawn over the output characteristic curve, makes contact at a point called as **Operating point**.

This operating point is also called as **quiescent point** or simply **Q-point**. There can be many such intersecting points, but the Q-point is selected in such a way that irrespective of AC signal swing, the transistor remains in active region. This can be better understood through the figure below.

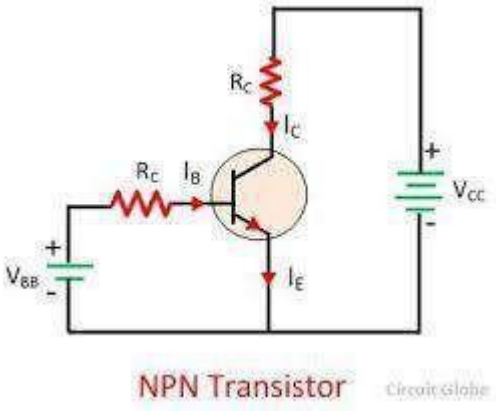


The load line has to be drawn in order to obtain the Q-point. A transistor acts as a good amplifier when it is in active region and when it is made to operate at Q-point, faithful amplification is achieved.

Faithful amplification is the process of obtaining complete portions of input signal by increasing the signal strength. This is done when AC signal is applied at its input.

DC Load line

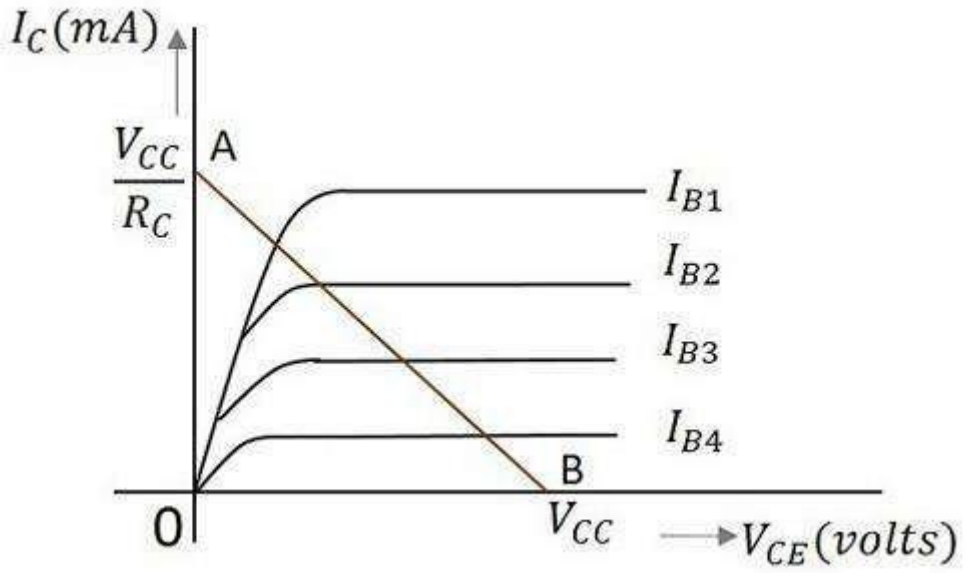
When the transistor is given the bias and no signal is applied at its input, the load line drawn at such condition, can be understood as **DC** condition. Here there will be no amplification as the AC signal is absent. The circuit will be as shown below.



The value of collector emitter voltage at any given time will be

$$V_{CE}=V_{CC}-I_CR_C$$

As V**CC** and R**C** are fixed values, the above one is a first degree equation and hence will be a straight line on the output characteristics. This line is called as **D.C. Load line**. The figure below shows the DC load line.



To obtain the load line, the two end points of the straight line are to be determined.Let those two points be A and B.

To obtain A

When collector emitter voltage VCE = 0, the collector current is maximum and is equal to VCC/RC. This gives the maximum value of VCE. This is shown as

$$V_{CE}=V_{CC}-I_CR_C$$

$$0=VCC-ICRC$$

$$IC=VCC/RC$$

This gives the point A (OA = VCC/RC) on collector current axis, shown in the abovefigure.

To obtain B

When the collector current IC = 0, then collector emitter voltage is maximum and willbe equal to the VCC. This is shown as

$$V_{CE}=V_{CC}-I_CR_C$$

$$Vce=VCC$$

(As Ic = 0)

This gives the point B, which means (OB = **VCC**) on the collector emitter voltage axis shown in the abovefigure.

Hence we got both the saturation and cutoff point determined and learnt that the load line is a straight line. So, a DC load line can be drawn.

Field Effect Transistor (FET)

Field-Effect Transistor (FET) is a semiconductor device that consists of a channel made of a semiconductor material, with two electrodes connected at either end, namely the drain and the source. The flow of current between the source and the drain terminals is controlled by a third electrode, known as the gate, which is placed in close proximity to the channel. By applying a voltage at the gate terminal, the number of charge carriers in the channel can be modulated, leading to a corresponding change in the current flow between the source and the drain terminals. The FET is classified into two types based on its mode of operation, namely the enhancement mode and depletion mode FETs, depending on whether the voltage applied at the gate terminal increases or decreases the current flow through the channel.

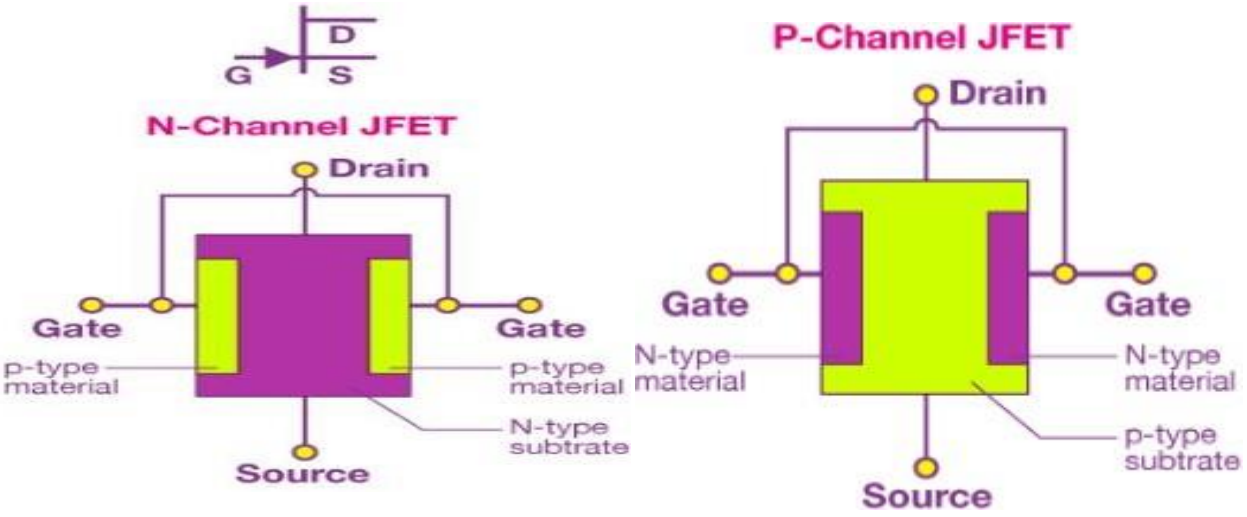
Types of FETs

There are two types of Field Effect Transistors:

- Junction Field Effect Transistor (JFET)
- Metal oxide semiconductor Field Effect Transistor (MOSFET)

JFET Construction

JFET is one of the most basic forms of field-effect transistors. They are three-terminal semiconductor electrical devices that can act as electronically controlled resistors or switches. Unlike a BJT (bipolar junction transistor), a JFET is voltage-controlled and does not require a biasing electrical current. The full-form JFET is Junction-gate Field Effect Transistor. The JFET controls the current flow between the source and the drain terminals by varying the voltage applied to the gate terminal. When a voltage is applied to the gate terminal, it creates an electric field that controls the width of the depletion region in the channel between the source and the drain terminals.



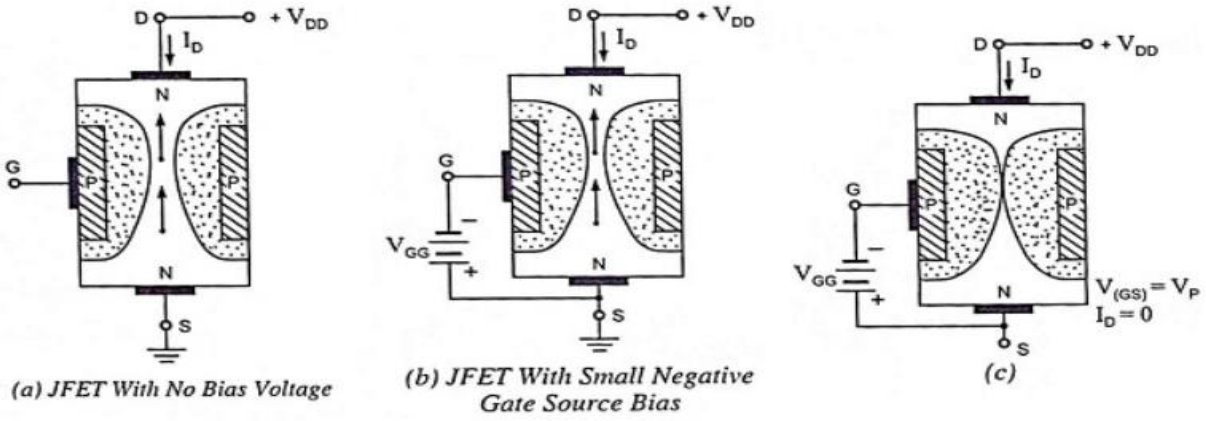
In an N-channel JFET, the material is of P-type, and the substrate is N-type, while in a P channel JFET the material is of N-type, and the substrate used is p-type. JFET is made of a long channel of semiconductor material. Ohmic contacts are provided at each end of the semiconductor channels to form source and drain connections. A P-type JFET contains many positive charges, and if the JFET contains a large number of electrons, it is called an N-type JFET.

JFET Operation

Let us understand the working of JFET by comparing it to a garden hose pipe. Water flows smoothly through a garden hose pipe if there is no obstruction, but if we squeeze the pipe slightly, the water flow slows down. This is precisely how a JFET works. Here the hose is analogous to JFET, and the water flow is equivalent to a current. By constructing the current carrying-channel according to our needs, we could control the current flow.

When neither any bias is applied to the gate (i.e. when $V_{GS} = 0$) nor any voltage to the drain w.r.t. source (i.e. when $V_{DS} = 0$), the depletion regions around the P-N junctions are of equal thickness and symmetrical.

(ii) When positive voltage is applied to the drain terminal D w.r.t. source terminal S without connecting gate terminal G to supply, as illustrated in Fig, the electrons (which are the majority carriers) flow from terminal S to terminal D whereas conventional drain current I_D flows through the channel from D to S. Due to flow of this current, there is a uniform voltage drop across the channel resistance as we move from terminal D to terminal S. This voltage drop reverse biases the diode. The gate is more negative with respect to those points in the channel which are nearer to D than to S. Hence, depletion layers penetrate more deeply into the channel at points lying closer to D than to S. Thus wedge-shaped depletion regions are formed, as shown in Fig. 13.6(a), when V_{DS} is applied. The size of the depletion layer formed determines the width of the channel and hence the magnitude of current I_D flowing through the channel.



(a) JFET With No Bias Voltage

(b) JFET With Small Negative Gate Source Bias

(c)

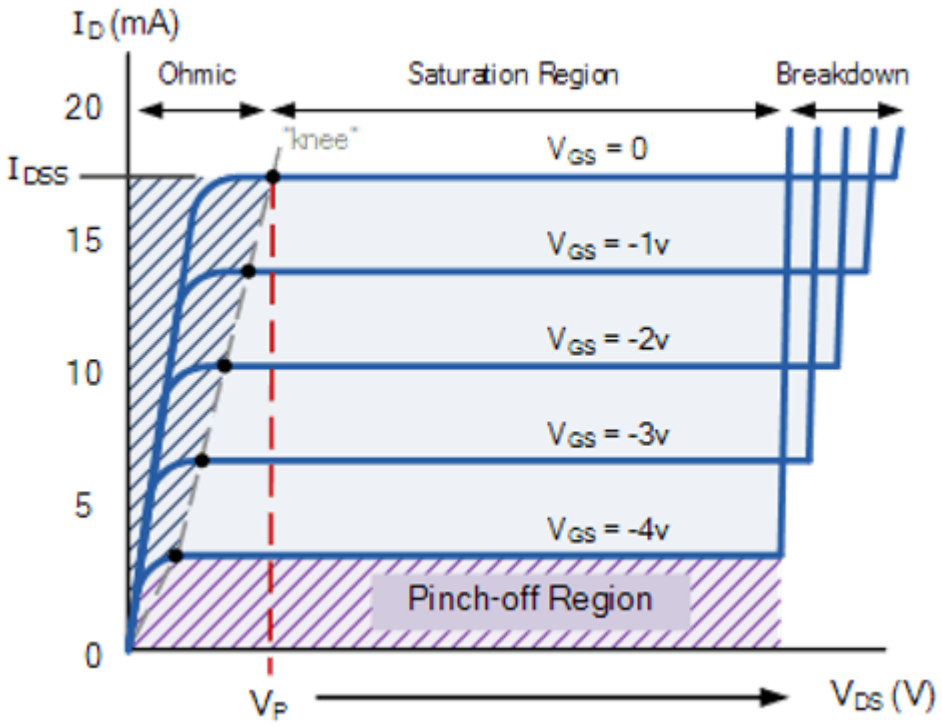
To see how the width of the channel varies with the variation in gate voltage, let us consider the situation when the gate is biased negative with respect to the source while the drain is applied

with positive bias with respect to the source, as illustrated in Fig. Now the P-N junctions are reverse biased and depletion regions are formed. P-regions are heavily doped compared to the N-channel, so the depletion regions penetrate deeply into the channel. Since a depletion region is a region depleted of the charge carriers, it behaves as an insulator. The result is that the channel is narrowed, the resistance is increased and drain current I_D is reduced. If the negative voltage at the gate is further increased, depletion layers meet at the centre and the drain current I_D is cut off completely. On the other hand, if the negative bias to the gate is reduced, the width of the depletion layers gets reduced causing decrease in resistance and, therefore, increase in drain current I_D. The gate-source voltage V_{GS} at which drain current I_D is cut off completely (pinched off), is called the **pinch-off voltage** V_P. It is also to be noted that

1. The amount of reverse bias is not the same throughout the length of the P-N junction. When the drain current flows through the channel, there is a voltage drop along its length. The result is that the reverse bias at the drain end is more than that at the source end making the width of depletion layer more at the drain end than that at the source end. Thus the channel becomes narrower at the drain end in comparison to that at source end, as shown in Fig.
2. The channel is not completely closed at the drain end. Because in that case there will be no drain current, so there will be no voltage drop along the channel length and amount of reverse bias will become uniform and the wedge shaped depletion region will become rectangular one. The channel will open and the drain current will flow. However, at pinch-off voltage, the channel width is reduced to a constant minimum value to allow the flow of drain current.
3. The N-channel JFET behaves as a vacuum tube triode. The drain and source perform the same functions as the plate and cathode, respectively and, like the grid of a triode, the Junction Field Effect Transistor gate controls the drain current. As is also the case with a grid, gate current is to be avoided, so the gate channel junctions are normally never forward biased.

The device is called the **field-effect transistor (FET)** because the drain current (output current) is controlled by the effect of the extension of the field associated with the depletion region developed by the reverse bias at the gate.

Output characteristic V-I curves of a N-Channel JFET



The voltage V_{GS} applied to the Gate controls the current flowing between the Drain and the Source terminals. V_{GS} refers to the voltage applied between the Gate and the Source while V_{DS} refers to the voltage applied between the Drain and the Source.

Because a **Junction Field Effect Transistor** is a voltage controlled device, "NO current flows into the gate!" then the Source current (I_S) flowing out of the device equals the Drain current flowing into it and therefore ($I_D = I_S$).

The characteristics curves example shown above, shows the four different regions of operation for a JFET and these are given as:

- Ohmic Region – When $V_{GS} = 0$ the depletion layer of the channel is very small and the JFET acts like a voltage controlled resistor.
- Cut-off Region – This is also known as the pinch-off region were the Gate voltage, V_{GS} is sufficient to cause the JFET to act as an open circuit as the channel resistance is at maximum.
- Saturation or Active Region – The JFET becomes a good conductor and is controlled by the Gate-Source voltage, (V_{GS}) while the Drain-Source voltage, (V_{DS}) has little or no effect.
- Breakdown Region – The voltage between the Drain and the Source, (V_{DS}) is high enough to causes the JFET's resistive channel to break down and pass uncontrolled maximum current.

The characteristics curves for a P-channel junction field effect transistor are the same as those above, except that the Drain current I_D decreases with an increasing positive Gate-Source voltage, V_{GS}.

The Drain current is zero when $V_{GS} = V_P$. For normal operation, V_{GS} is biased to be somewhere between V_P and 0. Then we can calculate the Drain current, I_D for any given bias point in the saturation or active region as follows:

Drain current in the active region.

$$I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]^2$$

Note that the value of the Drain current will be between zero (pinch-off) and I_{DSS} (maximum current). By knowing the Drain current I_D and the Drain-Source voltage V_{DS} the resistance of the channel (R_{DS}) is given as:

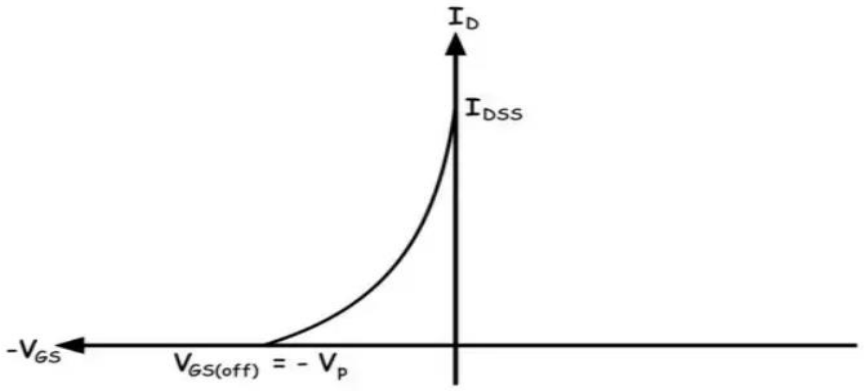
Drain-Source Channel Resistance.

$$R_{DS} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{g_m}$$

Where: g_m is the "transconductance gain" since the JFET is a voltage controlled device and which represents the rate of change of the Drain current with respect to the change in Gate-Source voltage.

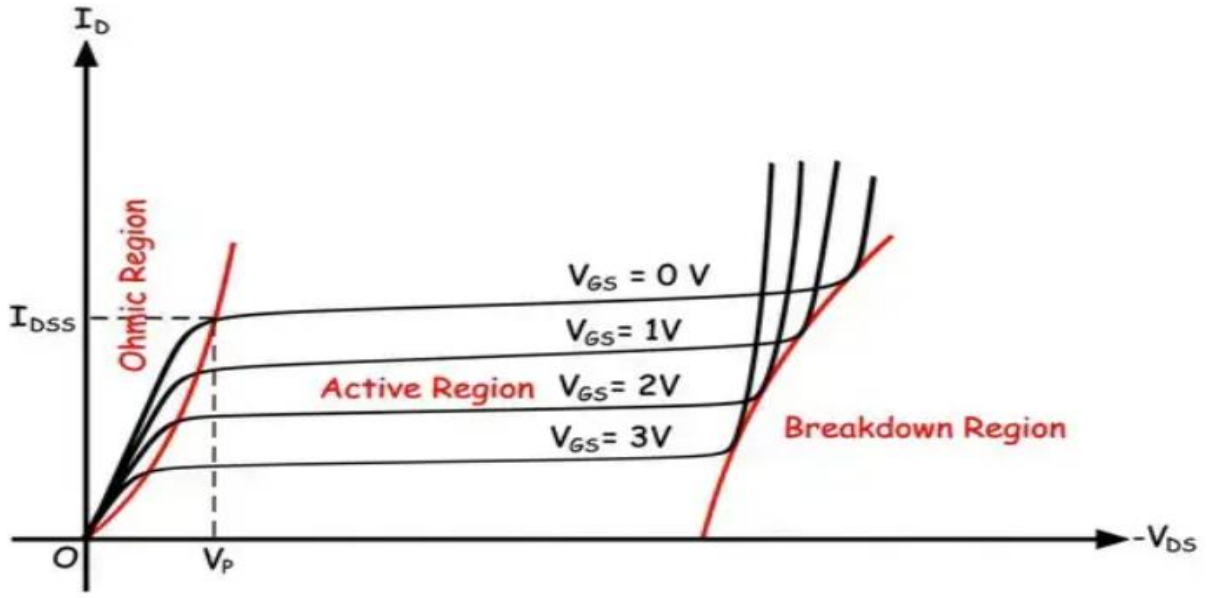
Transfer Characteristic of N Channel JFET

The transfer characteristic is drawn between gate voltage and drain current by keeping drain to source voltage at pinch-off voltage. When the gate is in zero potential the maximum drain current flowing through the transistor is shorted gate drain current(I_{DSS}). Now as the negative potential of the gate increases the corresponding drain current get decreased. After a certain negative gate voltage, the drain current becomes zero. This negative gate terminal voltage at which drain current becomes zero for the applied drain to source voltage same as pinch-off voltage is called gate to source cut off voltage $V_{GS(off)}$.



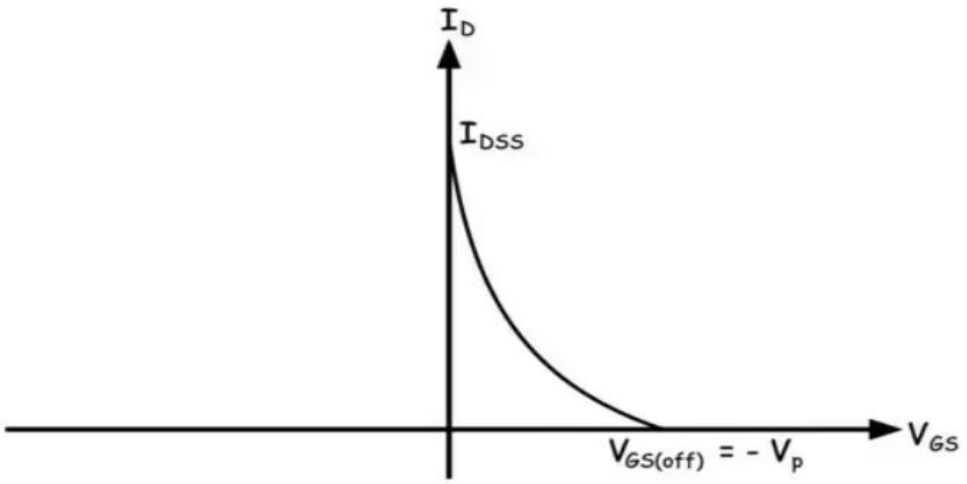
Output characteristic V-I curves of P Channel JFET

In p channel JFET we apply negative potential at drain terminal. If we make grounded both source and gate terminal and increase the negative potential of the drain from zero we will get the same curve as in the case of n channel JFET. Here at the beginning the drain current flowing from source to drain due to drift of holes in the same direction, linearly gets increased with increasing negative drain voltage. As the negative potential of the channel is more towards drain terminal hence the reverse biasing of the junction nearer to drain is more. This causes thicker depletion layer towards drain terminal. So just like the previous case the pinch-off occurs after certain negative drain voltage and the curve becomes horizontal. If we go on increasing negative drain voltage, after a certain negative drain voltage the depletion layers go through avalanche breakdown and the channel gets free from any further obstruction and drain current suddenly rises to a higher value. Hence, the curve will have a linear region at the beginning, an active region in the middle and breakdown region at the end. Now if we apply positive voltages at the gate terminal, the reverse biasing of the junction becomes more rapid and as a result, the characteristic curve gets shifted downward as shown below.



Transfer Characteristic of P Channel JFET

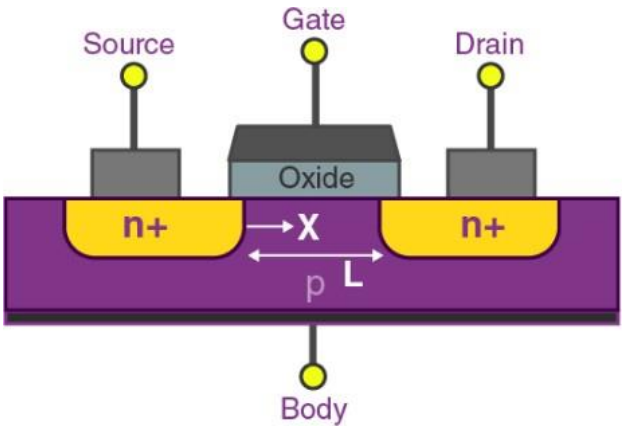
This is drawn between positive gate voltage and drain current. The pattern will be the same as in the case of n channel JFET but the polarity of the applied voltage and direction of the drain current differ.



Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET)

The MOSFET is another type of field-effect transistor (FET) that can switch electronic signals or amplify them. It is made of an insulated gate that controls the device's conductivity per the voltage applied. This nature makes it useful for switching electronic signals or amplifying by adjusting its conductivity with changing voltage levels.

The crucial advantage of MOSFET is that they require almost no input current to regulate the load current relative to bipolar transistors (BJTs or bipolar junction transistors). There are two types of MOSFETs: enhancement mode and depletion mode. In the case of an enhancement mode MOSFET, the exerted voltage at the gate increases the conductivity. In depletion mode transistors, the voltage exerted at the gate decreases the conductivity.



- The p-type semiconductor forms the base of the MOSFET.
- The two types of the base are highly doped with an n-type impurity which is marked as n+ in the diagram.
- From the heavily doped regions of the base, the terminals source and drain originate.
- The layer of the substrate is coated with a layer of silicon dioxide for insulation.
- A thin insulated metallic plate is kept on top of the silicon dioxide and it acts as a capacitor.
- The gate terminal is brought out from the thin metallic plate.
- A DC circuit is then formed by connecting a voltage source between these two n-type regions.

Depletion Mode

When there is no voltage across the gate terminal, the channel shows maximum conductance. When the voltage across the gate terminal is either positive or negative, then the channel conductivity decreases.

Enhancement Mode

When there is no voltage across the gate terminal, then the device does not conduct. When there is the maximum voltage across the gate terminal, then the device shows enhanced conductivity.

Operating Regions of MOSFET

A MOSFET is seen to exhibit three operating regions. Here, we will discuss those regions.

Cut-Off Region

The cut-off region is a region in which there will be no conduction and as a result, the MOSFET will be OFF. In this condition, MOSFET behaves like an open switch.

Ohmic Region

The ohmic region is a region where the current (I_{DS})increases with an increase in the value of V_{DS}. When MOSFETs are made to operate in this region, they are used as amplifiers.

Saturation Region

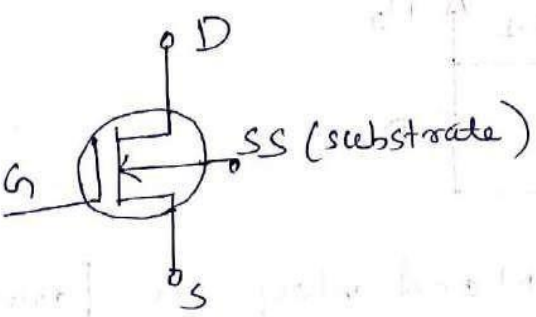
In the saturation region, the MOSFETs have their I_{DS} constant in spite of an increase in V_{DS} and occurs once V_{DS} exceeds the value of pinch-off voltage V_P. Under this condition, the device will act like a closed switch through which a saturated value of I_{DS} flows. As a result, this operating region is chosen whenever MOSFETs are required to perform switching operations.

MOSFET	BJT
There are two types of MOSFET and they are named: N-type or P-type	BJT is of two types and they are named as: PNP and NPN
MOSFET is a voltage-controlled device	BJT is a current-controlled device
The input resistance of MOSFET is high.	The input resistance of BJT is low.
Used in high current applications	Used in low current applications

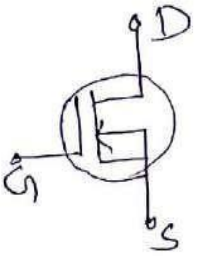
MOSFET:

Depletion type MOSFET symbol

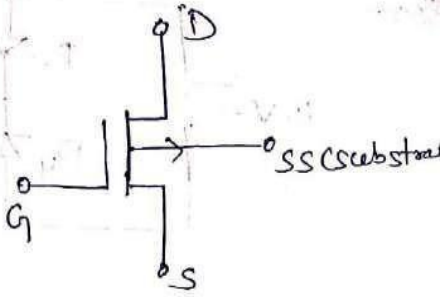
n channel



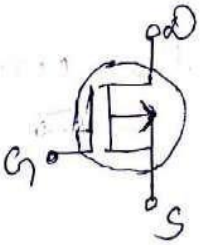
⇓ can be drawn



P channel

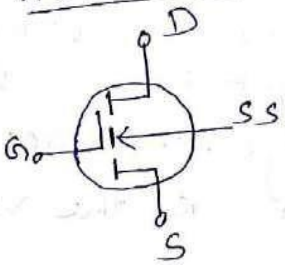


⇓ can be drawn



Enhancement type MOSFET symbol (Dashed line)

n channel



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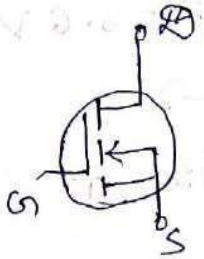
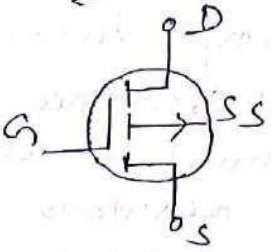


P channel



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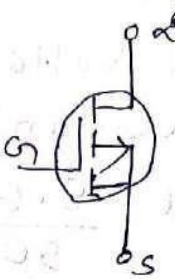


DMOSFET

i) Channel is available initially.

ii) Diffused channel

iii) Operates or can be operated in both Depletion & enhancement mode.

iv) Can be designed in Self biased arrangement.

v) Comparatively larger in size and expensive

vi) When $V_{GS}=0$, $I_D=I_{DSS}$

vii) No channel length modulation

EMOSFET

i) Channel is not present initially.

ii) Induced Channel

iii) Suitable for only Enhancement mode.

iv) Can't be designed in selfbiased arrangement.

v) Comparatively smaller in size, and economical for use.

vi) When $V_{GS}=0$, $I_D=0$

vii) Channel length modulation is there

MOSFET

(Metal Oxide Field Effect Transistor)

Mosfet has high input impedance and low cost of production as compared to JFET.

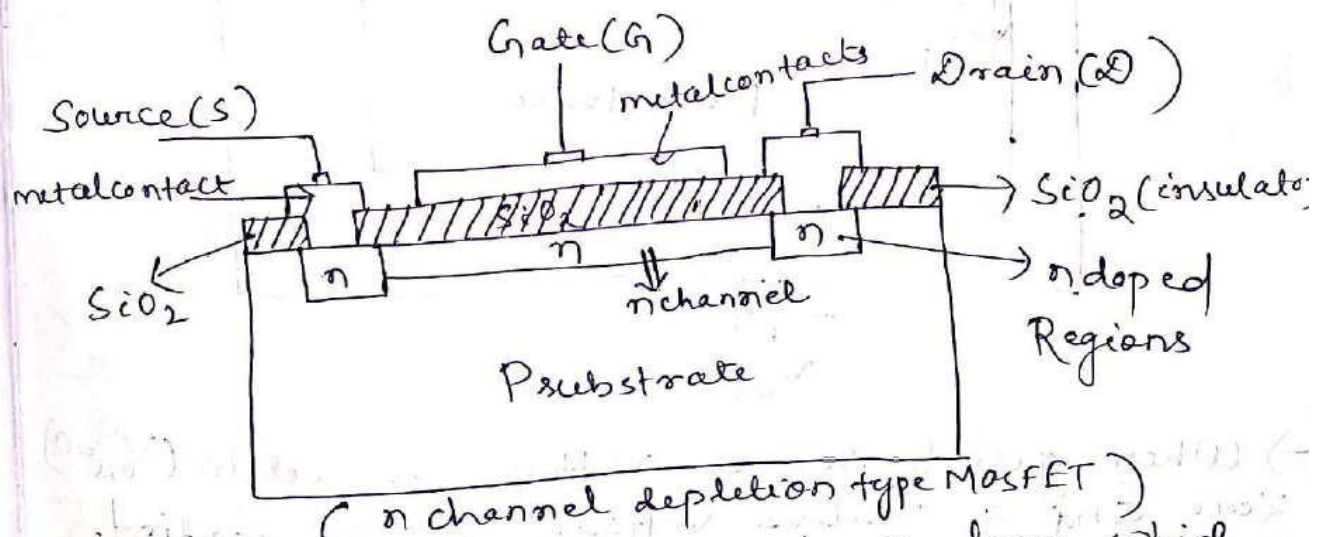
Types of MOSFET :—

1. Depletion-type MOSFET or DMOSFET → This mosfet can be operated in both Depletion mode & enhancement mode.
2. Enhancement-type MOSFET or EMOSFET → It can only be operated in enhancement mode.

→ MOSFET has four terminals :—

(i) Drain (ii) Gate (iii) Source (iv) Body or Substra

DEPLETION TYPE MOSFET :— (n channel)



(n channel depletion type MOSFET)

→ P type material is present as base which is referred to as substrate.

→ On some cases substrate is internally connected to the source terminal.

→ The source and drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel.

→ The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin silicon dioxide (SiO_2) layer.

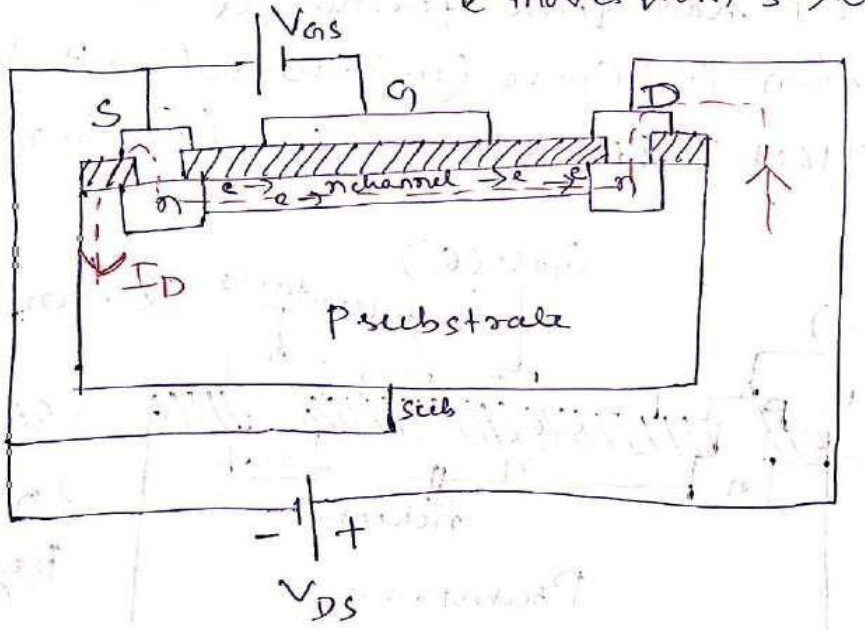
→ SiO_2 is a particular type of insulator referred to as a dielectric that sets up opposing electric fields within the dielectric when exposed to an externally applied field.

Basic Operation

V_{GS} = gate to source voltage

V_{DS} = drain to source voltage

I_D = Drain current (flows from D → S)
e⁻ moves from S → D



→ When gate-to-source voltage is set to ($V_{GS}=0$) zero and a positive voltage $V_{DS}>0$ is applied, then as drain is at more potential as compared to source, so, the result is an attraction for the positive potential at the drain by free electrons of the n channel.

→ When V_{GS} is set at negative voltage ($V_{GS} < 0V$) then the negative potential at the gate will tend to press the electrons towards the p-type substrate and will attract holes from the p-type substrate.

→ Depending on the magnitude of the negative bias established by V_{GS}, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the n-channel available for conduction.

→ The more negative the bias, the higher the rate of recombination. The resulting level of drain current is therefore reduced with increasing negative bias for V_{GS}.

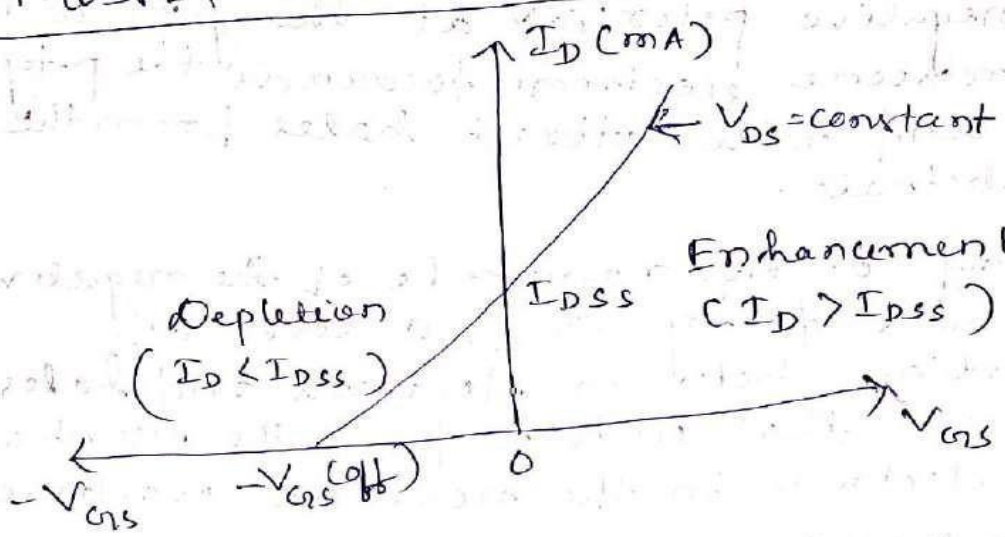
* For positive values of V_{GS}, the positive gate will draw additional electrons from the p-type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles.

→ With the V_{GS} increment in positive direction, the drain current will increase in rapid rate.

→ The positive gate-to-source voltage has "enhanced" the level of free carriers in the channel compared to $V_{GS} = 0V$.

→ For this reason the region of positive gate voltages on the drain or transfer characteristics is often referred to as the enhancement region, with the region between cutoff and saturation level of I_{DSS} referred to as the depletion region.

DMOSFET Characteristics :- (n channel)



(I_D Vs V_{GS}) ⇒ Transfer characteristic

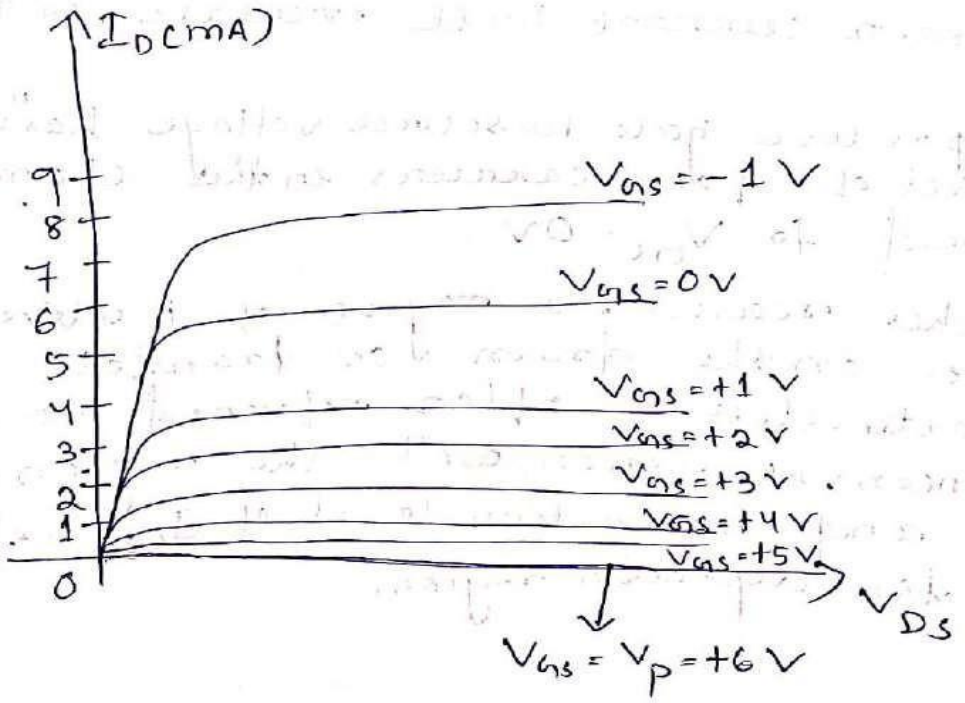
I_{DSS} is present when $V_{GS} = 0$ V

I_{DSS} = drain to source current with gate shorted ($V_{GS} = 0$)

I_D = Drain current

Characteristics :- (n channel)

I_D Vs V_{DS} when V_{GS} is applied :-



Shockley's equation for D-MOSFET :-

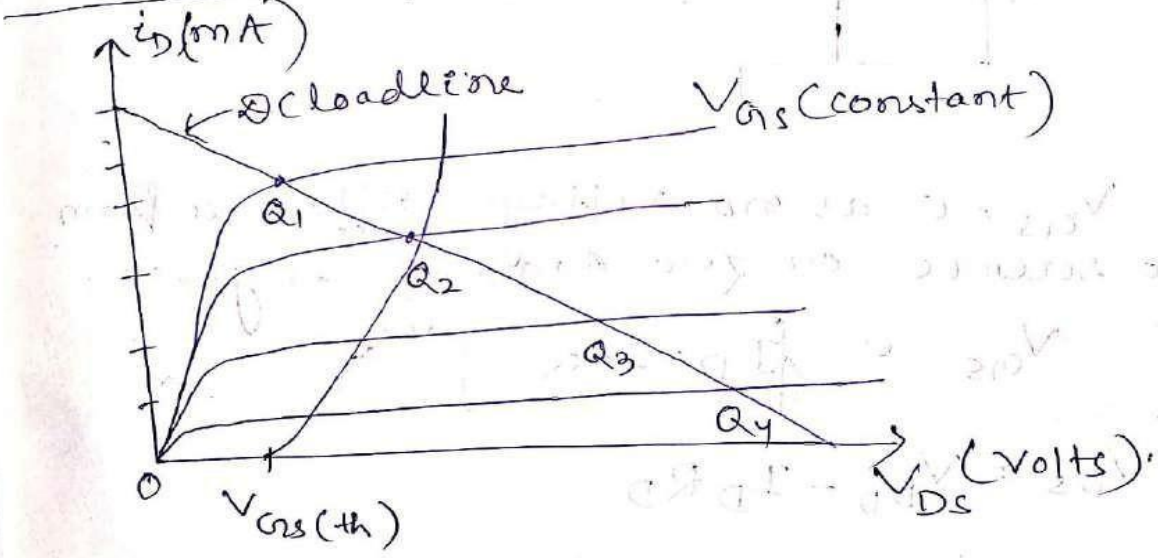
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

V_P = pinchoff voltage

Pinchoff refers to the threshold voltage below which the transistor turns off.

*. To get the Q point we have to get V_{GSQ} & I_{DQ} of MOSFET.

DC loadline & Q point



ENHANCEMENT-TYPE MOSFET (N Channel)

→ The construction of EMOSFET is similar to that of DMOSFET but here no channel (n type) is not present initially in between two n-doped regions. (*For construction refer to DMOSFET and here no channel is present initially)

→ The SiO_2 layer is present to isolate the gate metallic platform from the region between the drain and source.

Operation:-

→ If $V_{GS} = 0V$ and a voltage is applied between the drain and source of the device due to the absence of an n channel (absence of free carriers in between drain & source) and it will result in no current from D → S but we are getting $I_D = I_{DSS}$ when $V_{GS} = 0$ V in case of DMOSFET as channel is initially present.

→ With $V_{DS}, V_{GS} > 0V$, establishing the drain and gate at a positive potential w.r.t. the source.

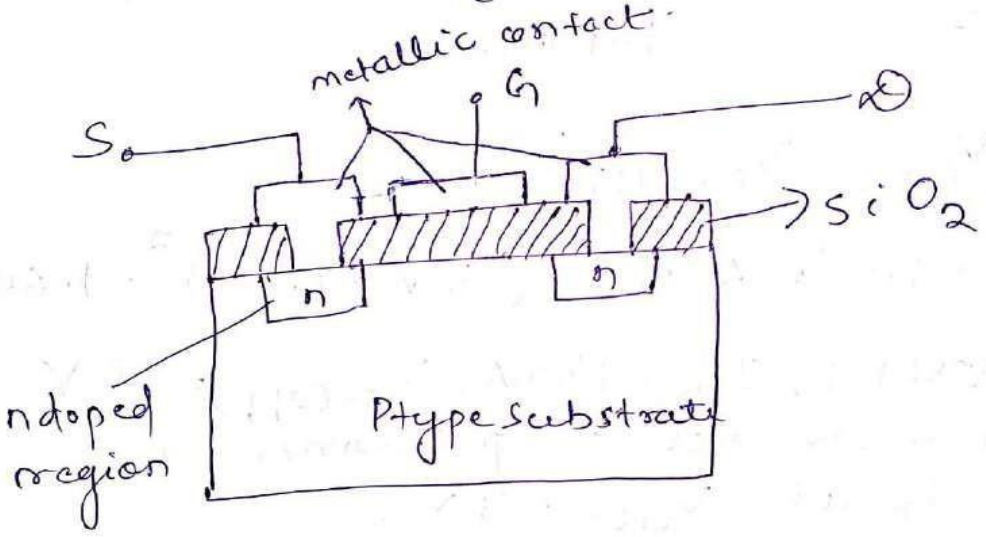
→ The positive potential at the gate will pressure the holes in the p substrate along the edge of SiO_2 layer to leave the area and enter deeper regions of 'p' substrate.

→ The result is a depletion region near the SiO_2 insulating layer void of holes. The e^- in the p-substrate (minority carriers) will be attracted to the positive gate and accumulate in the region near the surface of SiO_2 layer.

→ The SiO_2 insulating layer will prevent the negative carriers from being absorbed at the gate terminal.

→ As V_{GS} increases in magnitude, the concentration of e^- near the SiO_2 surface increases until the induced n-type region can support a measureable flow between drain & source.

n channel Enhancement MOSFET :—
(no channel initially)



→ The level of V_{GS} that results in significant increase in drain current is called as 'THRESHOLD VOLTAGE' and symbol is V_T.

→ At $V_{GS} = 0V$ no channel is present and channel is enhanced by $V_{GS} > 0V$, so this is called as ENHANCEMENT-type MOSFET.

→ If we hold V_{GS} constant and increase the level of V_{DS}, drain current will reach a saturation level

→ $\boxed{V_{DG} = V_{DS} - V_{GS}}$ (as source is connected to -ve)

→ If V_{DS} is increased and V_{GS} is held constant then V_{DG} also increases that means drain is at more potential w.r.t gate.

→ The saturation value of V_{DS} is related to V_{GS} by:

$$\boxed{V_{DS(sat)} = V_{GS} - V_T}$$

→ So current (I_D) increases when $V_{GS} > V_T$ so,

$$\boxed{I_D = k(V_{GS} - V_T)^2} \quad -\text{Imp.}$$

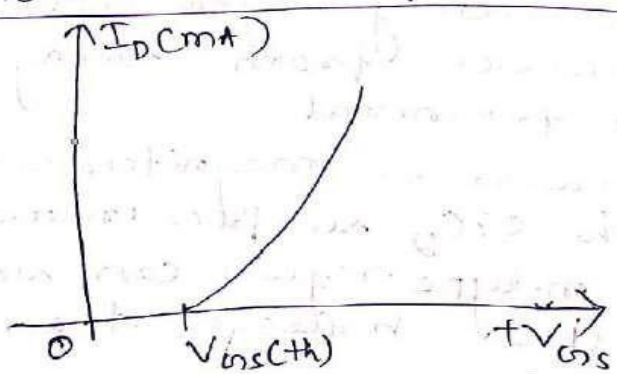
k = constant that is a function of construction of the device.

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

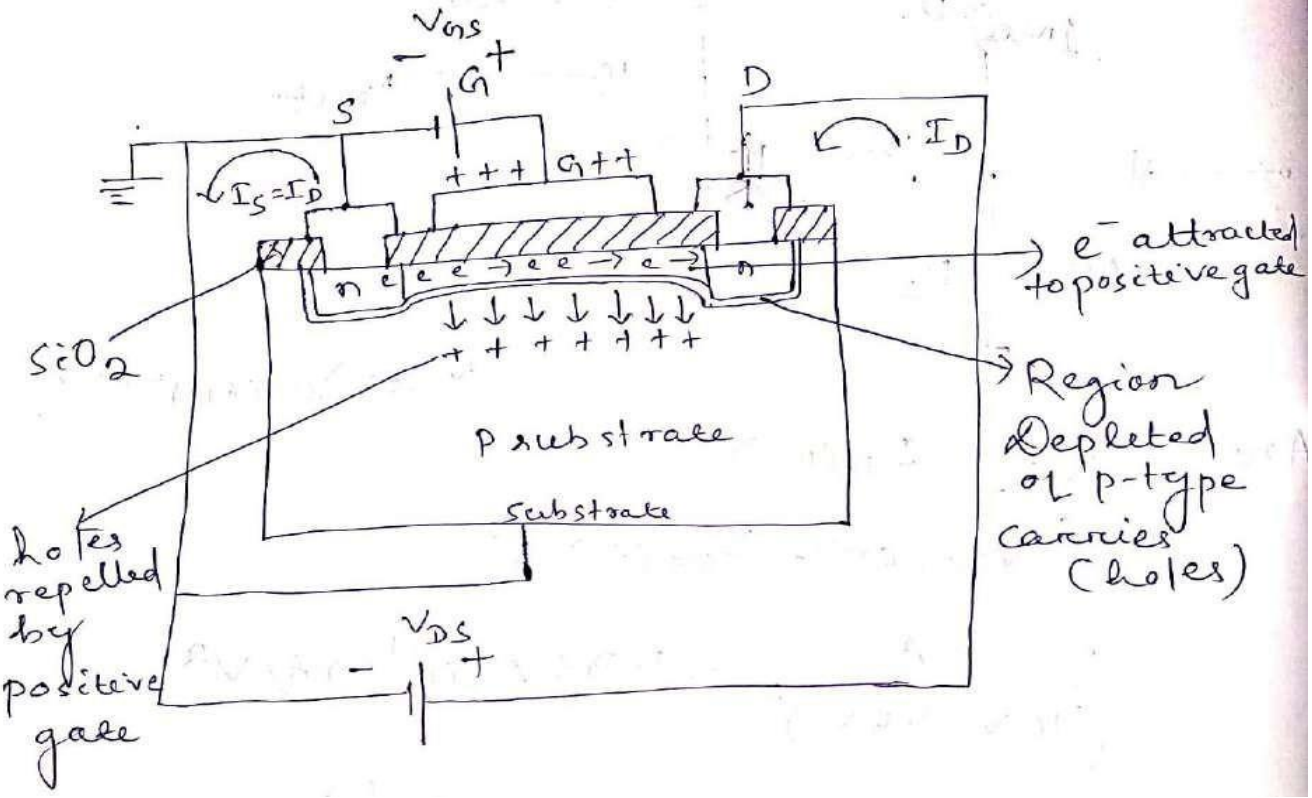
*. So here I_D & V_{GS} are in nonlinear relationship

EMOSFET n-channel transfer characteristics:-

I_D Vs V_{GS} :-



Enhancement n channel MOSFET with V_{GS} & V_{DS}:-



I_D V_s V_{DS} (n channel EMOSFET) (Drain characteristics)