

(Accredited by NBA, New Delhi. Validity 01.07.2022 to 30.06.2025)

**COURSE MODULE**

Academic Year: <b>2023-24</b>							
Department: <b>Electronics and Communication Engineering</b>							
Course Code	Course Title	Core/Elective	Prerequisite	Contact Hours			Total Hrs/ Sessions
				L	T	P	
BBEE203	Basic Electronics	Core	<b>Knowledge about the Semiconductor, BJT, logic gates and communication system</b>	<b>3</b>	<b>0</b>	<b>0</b>	<b>50</b>
<p><b>Course objectives:</b> Students will be taught</p> <ul style="list-style-type: none"> <li>• Operation of Semiconductor diode, Zener diode and Special purpose diodes and their applications.</li> <li>• Biasing circuits for transistor (BJT) as an amplifier.</li> <li>• Study of linear Op-amps and its applications.</li> <li>• Logic circuits and their optimization.</li> <li>• Principles of Transducers and Communication.</li> </ul>							
<b>Topics Covered as per Syllabus</b>							
<p><b>Module 1</b></p> <p><b>Semiconductor Diodes:</b> Introduction, PN Junction diode, Characteristics and Parameters, Diode Approximations, DC Load Line analysis (Text 1: 2.1,2.2,2.3,2.4)</p> <p><b>Diode Applications:</b> Introduction, Half Wave Rectification, Full Wave Rectification, Full Wave Rectifier Power Supply: Capacitor Filter Circuit, RC <math>\pi</math> Filter (includes numerical) (Text 1: 3.1,3.2,3.4,3.5)</p> <p><b>Zener Diodes:</b> Junction Breakdown, Circuit Symbol and Package, Characteristics and Parameters, Equivalent Circuit, Zener Diode Voltage Regulator. (Text1:2.9, 3.7).</p> <p><b>Module 2</b></p> <p><b>Bipolar Junction Transistors:</b> Introduction, BJT Voltages &amp; Currents, BJT Amplification, Common Base Characteristics, Common Emitter Characteristics, Common Collector Characteristics, BJT Biasing: Introduction, DC Load line and Bias point (Text 1: 4.2, 4.3, 4.5,4.6, 5.1)</p> <p><b>Field Effect Transistor:</b> Junction Field Effect Transistor, JFET Characteristics, MOSFETs: Enhancement MOSFETs, Depletion Enhancement MOSFETs (Text 1: 9.1,9.2,9.5)</p> <p><b>Module 3</b></p> <p><b>Operational Amplifiers:</b> Introduction, The Operational Amplifier, Block Diagram Representation of Typical Op-Amp, Schematic Symbol, Op-Amp parameters - Gain, input resistance, Output resistance, CMRR, Slew rate, Bandwidth, input offset voltage, Input bias Current and Input offset Current, The Ideal</p>							

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Op-Amp, Equivalent Circuit of Op-Amp, Open Loop Op-Amp configurations, Differential Amplifier, Inverting & Non Inverting Amplifier

**Op-Amp Applications:** Inverting Configuration, Non-Inverting Configuration, Differential Configuration, Voltage Follower, Integrator, Differentiator (Text 2: 1.1, 1.2, 1.3, 1.5, 2.2, 2.3, 2.4, 2.6, 6.5.1, 6.5.2, 6.5.3, 6.12, 6.13).

#### **Module 4**

**Boolean Algebra and Logic Circuits:** Binary numbers, Number Base Conversion, octal & Hexa Decimal Numbers, Complements, Basic definitions, Axiomatic Definition of Boolean Algebra, Basic Theorems and Properties of Boolean Algebra, Boolean Functions, Canonical and Standard Forms, Other Logic Operations, Digital Logic Gates (Text 3: 1.2, 1.3, 1.4, 1.5, 2.1, 2.2, 2.3, 2.4, 2.5, 2.6, 2.7)

**Combinational logic:** Introduction, Design procedure, Adders- Half adder, Full adder (Text 3: 4.1, 4.2, 4.3)

#### **Module 5**

**Introduction to Transducers:** Introduction, Resistive Transducers, Inductive Transducers, Capacitive Transducers, Thermal transducers, Optoelectronic transducer, and Piezoelectric transducers (Text 4: Chapter 18: 18.1, 18.2, 18.3, 18.4, 18.5)

**Communications:** Introduction to communication, Communication System, Modulation (Text book 5: 1.1, 1.2, 1.3)

#### **List of Text Books**

1. Electronic Devices and Circuits, David A Bell, 5<sup>th</sup> Edition, Oxford, 2016
2. Op-amps and Linear Integrated Circuits, Ramakanth A Gayakwad, Pearson Education, 4<sup>th</sup> Edition
3. Digital Logic and Computer Design, M. Morris Mano, PHI Learning, 2008 ISBN-978-81-203-0417
4. Electronic Instrumentation and Measurements (3rd Edition) – David A. Bell, Oxford University Press, 2013
5. Electronic Communication Systems, George Kennedy, 4<sup>th</sup> Edition, TMH

#### **List of URLs, Text Books, Notes, Multimedia Content, etc**

1. <https://nptel.ac.in/courses/122106025>
2. <https://nptel.ac.in/courses/108105132>
3. <https://nptel.ac.in/courses/117104072>

#### **Course Outcomes (Course Skill Set): Students will be able to**

1. **Develop** the basic knowledge on construction, operation and characteristics of semiconductor devices. (Level: C3)
2. **Apply** the acquired knowledge to construct small scale circuits consisting of semiconductor devices (Level: C3)
3. **Develop** competence knowledge to construct basic digital circuit by make use of basic gate and its function. (Level: C3)
4. **Construct** the conceptual blocks for basic communication system. (Level: C3)
5. **Apply** the knowledge of various transducers principle in sensor system. (Level: C3)

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### Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). The minimum passing mark for the SEE is 35% of the maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination(SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

#### Continuous Internal Evaluation(CIE):

Three Tests each of 20 Marks;

- 1<sup>st</sup>, 2<sup>nd</sup>, and 3<sup>rd</sup> tests shall be conducted after completion of the syllabus of 30-35%, 70-75%, and 90-100% of the course/s respectively.
- Assignments/Seminar/quiz/group discussion /field survey & report presentation/ course project/Skill development activities, suitably planned to attain the COs and POs for a total of 40 Marks.

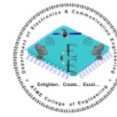
If the nature of the courses requires assignments/Seminars/Quizzes/group discussion two evaluation components shall be conducted. If course project/field survey/skill development activities etc then the evaluation method shall be one.

Total CIE marks (out of 100 marks) shall be scaled down to 50 marks

#### Semester End Examination(SEE):

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

- The question paper shall be set for 100 marks. The medium of the question paper shall be English). The duration of SEE is 03 hours.
- The question paper will have 10 questions. Two questions per module. Each question is set for 20 marks.The students have to answer 5 full questions, selecting one full question from each module. The student has to answer for 100 marks and **marks scored out of 100 shall be proportionally reduced to 50 marks.**
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.



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**The Correlation of Course Outcomes (CO's) and Program Outcomes (PO's)**

Cos/P Os	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
<b>CO1</b>	3	3	2	-	2	2						
<b>CO2</b>	3	2	3	-	2	1						
<b>CO3</b>	3	2	3	-	3				1			
<b>CO4</b>	2	1	1	-	2	1			1			1
<b>CO5</b>	2	1	1	-	2	1			1			1

**Note:** 3 = Strong Contribution 2 = Average Contribution 1 = Weak Contribution - = No Contribution